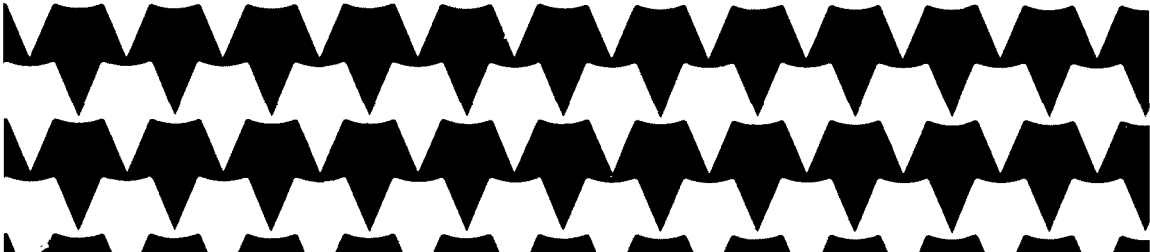
Cat. No. 25-1510

Tandy 1000EX

Technical Reference Manual



TANDY®

TANDY 1000 EX
TECHNICAL REFERENCE MANUAL

Tandy 1000 EX Technical Reference Manual
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MAIN LOGIC BOARD
POWER SUPPLIES
KEYBOARD
MEMORY PLUS
RS-232 INTERFACE BOARD
MOUSE CONTROLLER/CALENDAR
PLUS NETWORK 4 INTERFACE
DEVICES

Note: Complete information for the Disk Drives for this unit is available through your local store. They will order the desired Service Manual from Radio Shack National Parts, Fort Worth, Texas.

Foldout Page Insertion Guide

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Light Blue To System Timing Diagram	Sheets 1 of 2 and 2 of 2
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MAIN LOGIC BOARD

MAIN LOGIC BOARD
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INTRODUCTION TO THE TANDY 1000 EX COMPUTER

The Tandy 1000 EX Computer is modular in design to allow maximum flexibility in system configuration. The computer consists of a Main Unit, and a monitor. The Main Unit is supplied with one internal floppy disk drive. A second external floppy disk drive is optional. Each disk drive has a capacity of 360K bytes formatted. The standard types of monitors used with the Tandy 1000 EX are the monochrome composite and the color RGB monitor. Since these units are modular, they may be placed on top of the Main Unit or at any convenient location.

The Tandy 1000 EX has a standard 256K of system RAM. An optional DMA/RAM board allows the Tandy 1000 EX to be expanded by 128K or 384K of RAM. This board will fit onto the expansion slot. With a fully populated RAM board installed, the Tandy 1000 EX will have 640K bytes of RAM allowed by the system memory map.

Other features include a parallel printer port, two built-in joystick interfaces, and a speaker for audio feedback.

The Main Unit is the heart of the Tandy 1000 EX. It houses the Main Logic Assembly, system power supply, floppy disk drive, and keyboard.

The Main Logic Assembly is a large board mounted to the bottom of the Main Unit and interconnected to the keyboard, power supply, and disk drive by a series of cables. Figure 1 shows the Tandy 1000 EX.

The Power Supply is a 28W switching regulator type, designed to provide adequate power capacity for a fully configured system.

The Floppy Disk Drive uses double-sided, double-density diskettes to read, write, or store data. These are soft sector diskettes. The Disk Drive assembly is installed in the standard unit. All system programs, with the exception of the system startup sequence, are stored on disk.

Either a monochrome or a color display may be used with the Tandy 1000 EX. The monochrome monitor is a high-resolution green phosphor display which provides excellent visual quality. It features a 12" screen with an anti-glare surface. Each display is capable of 25 lines of 80 characters. The character matrix is 8 wide x 9 high.

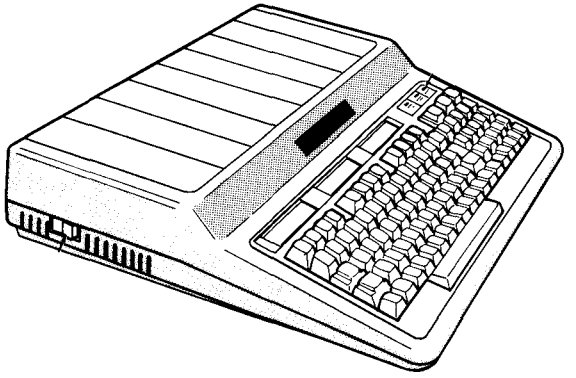


Figure 1. TANDY 1000 EX

SPECIFICATIONS

Processor: Intel 8088

Dimensions: 3 1/4 x 17 x 14 1/2 (HWD)

Weight: 11 lbs

Power Requirements: 120 VAC, 60 Hz

With Floppy Disk Drives, Memory Cards, and RS-232:
AC Current: 0.7 - 0.8 Amps with Floppy doing R/W tests.
Leakage Current: 0.5 mA
+5 VDC 3.0 Amps max., 1.9 Amps Typ.
+12 VDC 2.0 Amps max. 1.2 Amps continuous
-12 VDC .1 Amp max.

Environment:
Air Temperature
System ON: 60 to 90 degrees F (15.6 to 32.2 degrees C)
System OFF: 50 to 110 degrees F (10 to 43 degrees C)
Humidity: System ON-OFF: 8% to 80%

Disk Drive Specifications
Power:

Supply Voltage	+5 VDC Input	+12 VDC Input
Ripple 0 to 50 kHz	100 mV	200 mV
Tolerance Including Ripple	+/-5%	+/-10%
Standby Current Nominal	4 mA	0.2 mA
Standby Current Worst Case	6.8 mA	0.5 mA
Operating Current Nominal	170 mA	120 mA
Operating Current Worst Case	120 mA	230 mA

Environment:
Temperature
Operating 40 to 125 degrees F (4 to 51.5 C)
Nonoperating -40 to 149 degrees F (-40 to 65C)
Relative Humidity
Operating 20% to 80% (noncondensing)
Nonoperating 10% to 90% (noncondensing)

Connector Pin Assignments

J1 -- Speaker Interface
(2-Pin Vertical Header)

1 -- Sound	2 -- Ground

J2 -- PWR, NUM, CAP

1 -- Power Indicator	2 -- Gnd
3 -- Num Indicator	4 -- NUMLOCK Control
5 -- CAPS Indicator	6 -- CAPS Control

J3 -- Keyboard Interface

1 -- X1	7 -- X0
2 -- X5	8 -- X7
3 -- X4	9 -- X3
4 -- X3	10 -- X1
5 -- X2	11 -- X5
6 -- X6	12 -- X4

J5 -- Fan

1 -- +12V	2 -- GND

J6 -- DC POWER
(6-Pin Vertical Header)

1 -- +5 VDC	2 -- +5 VDC
3 -- GND	4 -- Ground
5 -- +12V	6 -- -12V

J7 -- Keyboard Interface

1 -- Y0	8 -- Y6
2 -- Y1	9 -- Y7
3 -- Y11	10 -- Y8
4 -- Y2	11 -- Y9
5 -- Y3	12 -- Y10
6 -- Y4	13 -- Y11
7 -- Y5	

J8 -- Audio Jack

1 -- GND	2 -- AUDIOOUT

J9 -- Right Joystick
(6-Pin Rt. Angle Circular Din)

1 -- Y Axis	2 -- X Axis
3 -- Ground	4 -- Switch 1
5 -- +5 VDC	6 -- Switch 2

J10 -- Left Joystick
(6-Pin Rt. Angle Circular Din)

1 -- Y Axis	2 -- X Axis
3 -- Ground	4 -- Switch 1
5 -- +5 VDC	6 -- Switch 2

J11 -- Floppy Disk Interface Internal
(Dual 17-Pin Vertical Header)

1 -- Ground	2 -- NC
3 -- Ground	4 -- NC
5 -- Ground	6 -- NC
7 -- Ground	8 -- INDEX*
9 -- Ground	10 -- DSINT*
11 -- Ground	12 -- NC
13 -- Ground	14 -- NC
15 -- Ground	16 -- MTRON*
17 -- Ground	18 -- DIR*
19 -- Ground	20 -- STEP*
21 -- Ground	22 -- WRDATA*
23 -- Ground	24 -- WEN*
25 -- Ground	26 -- TRK0*
27 -- Ground	28 -- WRPRT*
29 -- Ground	30 -- RDDATA*
31 -- Ground	32 -- SIDESELECT*
33 -- Ground	34 -- NC

J12 -- Expansion Interface Connectors
(Dual 31-Pin Header)

A01 -- NMI	B01 -- Ground
A02 -- D7	B02 -- RESET
A03 -- D6	B03 -- +5 VDC
A04 -- D5	B04 -- IR2
A05 -- D4	B05 -- NC
A06 -- D3	B06 -- FDCDMRQ*
A07 -- D2	B07 -- -12 VDC
A08 -- D1	B08 -- AUDIOIN
A09 -- D0	B09 -- +12 VDC
A10 -- RDYIN	B10 -- Ground
A11 -- AEN	B11 -- MEMW*
A12 -- A19	B12 -- MEMR*
A13 -- A18	B13 -- IOW*
A14 -- A17	B14 -- IOR*
A15 -- A16	B15 -- (DACK3*)
A16 -- A15	B16 -- (DRQ3*)
A17 -- A14	B17 -- (DACK1*)
A18 -- A13	B18 -- (DRQ1*)
A19 -- A12	B19 -- REFRESH*
A20 -- A11	B20 -- CLK
A21 -- A10	B21 -- RFSH
A22 -- A09	B22 -- BREQ*
A23 -- A08	B23 -- NC
A24 -- A07	B24 -- IR4
A25 -- A06	B25 -- IR3
A26 -- A05	B26 -- FDCDACK*
A27 -- A04	B27 -- DMATC
A28 -- A03	B28 -- ALE
A29 -- A02	B29 -- +5 VDC
A30 -- A01	B30 -- OSC
A31 -- A00	B31 -- Ground

J13 -- Parallel Interface
(34-Pin Header)

1 -- PPSTROBE*	2 -- Ground
3 -- PPDATA0	4 -- Ground
5 -- PPDATA1	6 -- Ground
7 -- PPDATA2	8 -- Ground
9 -- PPDATA3	10 -- Ground
11 -- PPDATA4	12 -- Ground
13 -- PPDATA5	14 -- NC
15 -- PPDATA6	16 -- Ground
17 -- PPDATA7	18 -- Ground
19 -- PPACK*	20 -- Ground
21 -- PPBUSY	22 -- Ground
23 -- PPPAEM	24 -- Ground
25 -- PPSEL*	26 -- NC
27 -- PPAUTOF*	28 -- PPFAULT
29 -- NC	30 -- PPINIT*
31 -- Ground	32 -- NC
33 -- Ground	34 -- NC

J14 -- Floppy Disk Interface External

1 -- +12V	2 -- +5V
3 -- +12V	4 -- +5V
5 -- GND	6 -- +5V
7 -- GND	8 -- +5V
9 -- GND	10 -- INDEX*
11 -- GND	12 -- TK0*
13 -- GND	14 -- STEP*
15 -- SIDESELECT*	16 -- MTRON*
17 -- DIR*	18 -- GND
19 -- WRPRT*	20 -- GND
21 -- RDDATA*	22 -- GND
23 -- WRDATA*	24 -- GND
25 -- WEN*	26 -- GND
27 -- NC	28 -- +12V
29 -- DSEXT*	30 -- +12V

J15 -- Composite Output
(Rt. Angle RCA-Type Phone Jack)

1 -- Compvid	2 -- Ground

J16 -- RGBI Video
(9-Pin Socket Rt. Angle D-Subminiature)

1 -- Ground	2 -- Ground
3 -- Red	4 -- Green
5 -- Blue	6 -- Intensity
7 -- Green (Monochrome Video)	8 -- HSYNC
9 -- VSYNC	

REVISION			
LTR	DESCRIPTION	DATE	APPD

SPECIFICATION - OPTION CARD

REFERENCE DRAWINGS
B1720019
D1720020
C1720011

MAT'L		DRAFT S. LONG	DATE 1/23/86	TITLE
		CHECK	DATE	
		DESIGN	DATE	SPECIFICATION OPTION CARD
FINISH		APPD	DATE	
		APPD	DATE	
		USED ON	TANDY	DWG. NO A-8080083
				SCALE / SHEET OF

NOTES (UNLESS OTHERWISE SPECIFIED):

DIM. ARE IN INCHES AND APPLY AFTER PLATING	TOLERANCE xx = ± .010 xxx = ± .005
DO NOT SCALE DWG.	ANGLES = ± 1°

Option Card Description

PINOUT:

IBM Bus Signal	Proj 620 Signal	PIN	PIN	Proj 620 SIGNAL	IBM Bus Signal
GND	GND	B01	A01	NMI	I/OCHCK*
RESETDRV	BRESET	B02	A02	D7	D7
+5V	+5V	B03	A03	D6	D6
IRQ2	IR2	B04	A04	D5	D5
-5VDC	NC	B05	A05	D4	D4
DRQ2	FDCDMARQ0*	B06	A06	D3	D3
-12V	-12V	B07	A07	D2	D2
Reserved	AUDIOIN	B08	A08	D1	D1
+12V	+12V	B09	A09	D0	D0
GND	GND	B10	A10	READY	I/OCHRDY
MEMW*	MEMW*	B11	A11	AEN	AEN
MEMR*	MEMR*	B12	A12	A19	A19
IOW*	IOW*	B13	A13	A18	A18
IOR*	IOR*	B14	A14	A17	A17
DACK3*	DACK3*	B15	A15	A16	A16
DRQ3	DRQ3*	B16	A16	A15	A15
DACK1*	DACK1*	B17	A17	A14	A14
DRQ1	DRQ1*	B18	A18	A13	A13
DACK0*	REFRESH*	B19	A19	A12	A12
CLOCK	CLK	B20	A20	A11	A11
IRQ7	RFSH*	B21	A21	A10	A10
IRQ6	BREQ*	B22	A22	A09	A09
IRQ5	NC	B23	A23	A08	A08
IRQ4	IR4	B24	A24	A07	A07
IRQ3	IR3	B25	A25	A06	A06
DACK2*	FDCDMACK*	B26	A26	A05	A05
T/C	TC	B27	A27	A04	A04
ALE	ALE	B28	A28	A03	A03
+5V	+5V	B29	A29	A02	A02
OSC	OSC	B30	A30	A01	A01
GND	GND	B31	A31	A00	A00

OSC	O	Oscillator: 14.31818 Mhz High-speed clock with a 50% duty cycle
CLK	O	System clock: It can be 4.77 Mhz with a 33% duty cycle or 7.16 Mhz with a 50% duty cycle.
BRESET	O	Buffered Reset: This line is used to reset or initialize system logic upon power-up or during a lowline voltage outage. This signal is synchronized to the falling edge of clock and is active high.
A0-A19	O	Address bits 0 to 19: These lines are used to address memory and I/O devices within the system. The 20address lines allow

		access of upto 1 megabyte of memory. A0 is the least significant (LSB) and A19 is the most significant (MSB). These lines are generated by either the processor or DMA controller. They are active high.
D0-D7	I/O	Data Bits 0 to 7: These lines provide data bus bits 0 to 7 for the processor, memory, and I/O devices. D0 is the least significant bit (LSB) and D7 is the most significant bit (MSB). These lines are active high.
ALE	O	Address Latch Enable: This line is provided by the Bus Controller and is used on the system board to latch valid addresses from the processor. It is available to the I/O channel as an indicator of a valid processor address (when used with AEN). Processor addresses are latched with the falling edge of ALE.
NMI	I	-Nonmaskable Interrupt: This line provides the processor with parity (error) information on memory or devices in the I/O channel. When this signal is active low, a parity error is indicated.
RDYIN	I	Ready In: This line, normally high (ready), is pulled low (not ready) by a memory or I/O device to lengthen I/O or memory cycles. It allows slower devices to attach to the I/O channel with a minimum of difficulty. Any slow device using this line should drive it low immediately upon detecting a valid address and a read or write command. This line should never be held low longer than 10 clock cycles. Machine cycles (I/O or memory) are extended by an integral number of CLK cycles (210ns).
IR2-IR4 BREQ, RFSH*	I	Interrupt Request: These lines are used to signal the processor that an I/O device requires attention. They are prioritized with IRQ2 as the highest priority and RFSH* as the lowest. An Interrupt Request is generated by raising an IRQ line (low to high) and holding it high until it is acknowledged by the processor (interrupt service routine).
IOR*	O	-I/O Read command: This command line instructs an I/O device to drive its data

		onto the data bus. It may be driven by the processor or the DMA controller. This signal is active low.
IOW*	O	-I/O Write command: This command line instructs an I/O device to read the data on the data bus. It may be driven by the processor or the DMA controller. This signal is active low.
MEMR*	O	Memory Read command: This command line instructs the memory to drive its data onto the data bus. It may be driven by the processor or the DMA controller. This signal is active low.
MEMW*	0	Memory Write command: This command line instructs the memory to store the data present on the data bus. It may be driven by the processor or the DMA controller. This signal is active low.
FDCDMRQ*	I	FDC DMA Request: This line is an asynchronous channel request used by a floppy disk to gain DMA service. A request is generated by bringing the line to an active level (high). The line must be held high until the FDCDACK* line goes active.
REFRESH* FDCDACK*	O	-DMA Acknowledge: These lines are used to acknowledge FDC DMA requests and to refresh system dynamic memory. They are active low.
AEN	O	Address Enable: This line is used to de-gate the processor and other devices from the I/O channel to allow DMA transfers to take place. When this line is active (high), the DMA controller has control of the address bus, data bus, read commnad lines (memory and I/O), and the write command lines (memory and I/O).
DMATC	O	Terminal Count: This line provides a pulse when the terminal count for any DMA channel is reached. This signal is active high.
AUDIOIN	I	Audio In: This line allows a peripheral device to generate sound using the internal speaker.
Voltages: +5Vdc+/-5%, 1.4A,		located on 2 connector pins (.45A per option board).

+12Vdc+/-5%, 0.1A,	located on 1 connector pin (0.03A per option board).
-12Vdc+/-10%, 0.1A,	located on 1 connector pin (0.03A per option board).
GND (Ground),	located on 3 connector pins

BUS INTERFACE SPECIFICATIONS

This specification is for the primary bus on the Tandy 1000 EX main logic board, which also is available to the option board connectors. The specification describes the signals in the following manner. See Figures 2 and 3.

- The following signal nomenclature is used in the schematic and literature. Signals designated with the suffix "*" are logically "true low" (normal inactive state is high); if they are not so designated, the signal is logically "true high."
- Direction -- input or output -- is referenced to the CPU.
- Brief functional description of the signal.
- Description of the "drive" or "load" characteristics of the signal. This includes the specific source by IC type and reference designator, drive capability for "output" signals, and actual load for "input" signals. The drive/load is defined in "unit loads" and specified as "high/low." This specification is for the main logic board only. Some signals have an alternate source, an external bus master such as the DMA.
- 1 Unit Load (UL) is defined as: Ioh = .04mA @ 2.4V
Iol = 1.6mA @ 0.5V

Signal Listing

A00 - A19	O	ADDRESS	SOURCE: U18,U19,U20 Drive - 65/15 UL Latch Strobe - ALE Output Enable - AEN Alternate external source
D0-D7	I/O	DATA	SOURCE: U13 Drive - 37/15 UL Direction Control - RD* (CPU read signal) Enable - DEN*
ALE	O	ADDRESS LATCH STROBE	SOURCE: U12
IOW*	O	I/O WRITE STROBE	Drive - 50/7.5 UL
IOR*	O	I/O READ STROBE	Output Enable - AEN
MEMW*	O	MEMORY WRITE STROBE	Pull-Up - 4.7K ohms

MEMR*	O	MEMORY READ STROBE	Alternate external source
CLK	O	CPU CLOCK	7.16MHz, 50% duty cycle or 4.77MHz, 33% duty cycle SOURCE: U18 Drive - 75/7.5 UL
OSC	O	OSCILLATOR	14.32MHz, 50% duty cycle SOURCE: U18 Drive - 75/7.5 UL
NMI	I	NON-MASKABLE INTERRUPT	To System NMI Load: 1/1 UL, U3
RDYIN	I	SYSTEM WAIT	SOURCE: OPEN-COLLECTOR OR 3-STATE BUFFERS Load: 1 UL and 1.0K ohm pull-up. 10/0.9 UL Set LOW by Peripherals (I/O or Memory) to extend READ or WRITE cycles.
RESET	O	SYSTEM RESET	Power On or Manual SOURCE: U18 Drive: 75/7.5 UL
BREQ*	I	BUS REQUEST	From external masters Load: 1 UL and 10K ohm pull-up. 10/0.9 UL
AEN	O	BUS GRANT	To external masters SOURCE: U18 Drive - 75/7.5 UL
IR2	I	INTERRUPT REQUEST#2	To system interrupt controller
IR3	I	INTERRUPT REQUEST#3	Load: 1 UL and 2.2K pull-down
IR4	I	INTERRUPT REQUEST#4	
AUDIO IN	I		Not Used.
AUDIO OUT	O		To External Source Drive: 1.25 Volts P-P into 10K

The following are not sourced by the CPU but are to be SOURCED (O) Output or Loaded (I) Input by an external DMA source:

RFSH	I	REQUEST DMA CHANNEL#0	Dedicated input requests to DMA
DRQ1	I	REQUEST DMA CHANNEL#1	
FDCDMRQ	I	REQUEST DMA CHANNEL#2	1 MOS load 40/160 UL
DRQ3	I	REQUEST DMA CHANNEL#3	
REFRESH*	O	ACKNOWLEDGE DRQ0*	Dedicated output acknowledges from DMA.
DACK1*	O	ACKNOWLEDGE DRQ1*	
FDCDACK*	O	ACKNOWLEDGE DRQ2*	
DACK3*	O	ACKNOWLEDGE DRQ3*	
DMATC	O	TERMINAL COUNT	Used by DMA Controller to indicate Terminal Count reached. Drive: 2/2 UL

+5VDC	+5VDC	4% 1.0 Amps available on the bus.
+12VDC	+12VDC	5% .3 Amps available on the bus.
-12VDC	-12VDC	+8.3% - 25% 0.06 Amps available on the bus.
GROUND	Power Return for +5, +12, -12 VDC.	

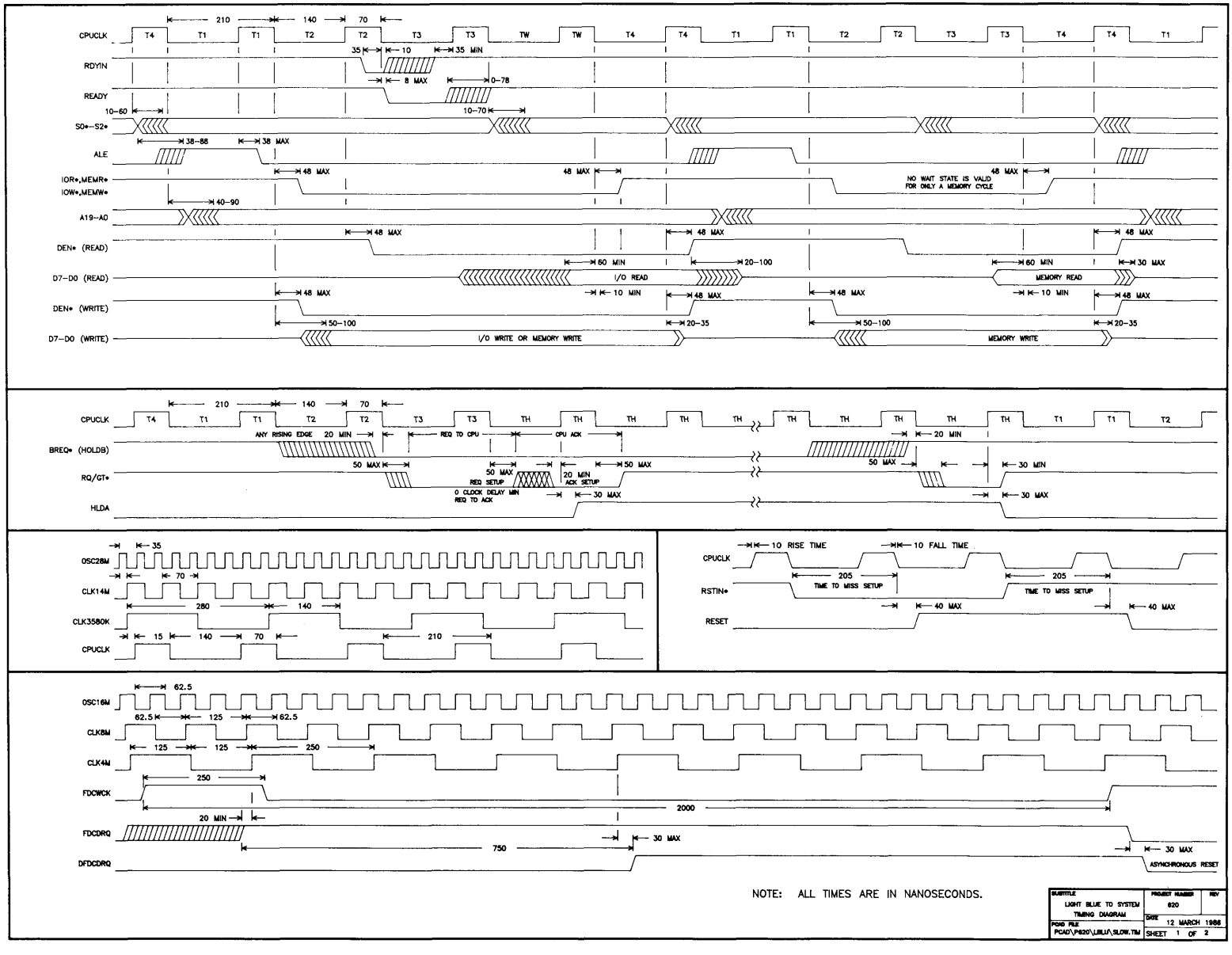


Figure 2. Light Blue to System Timing (1 of 2)

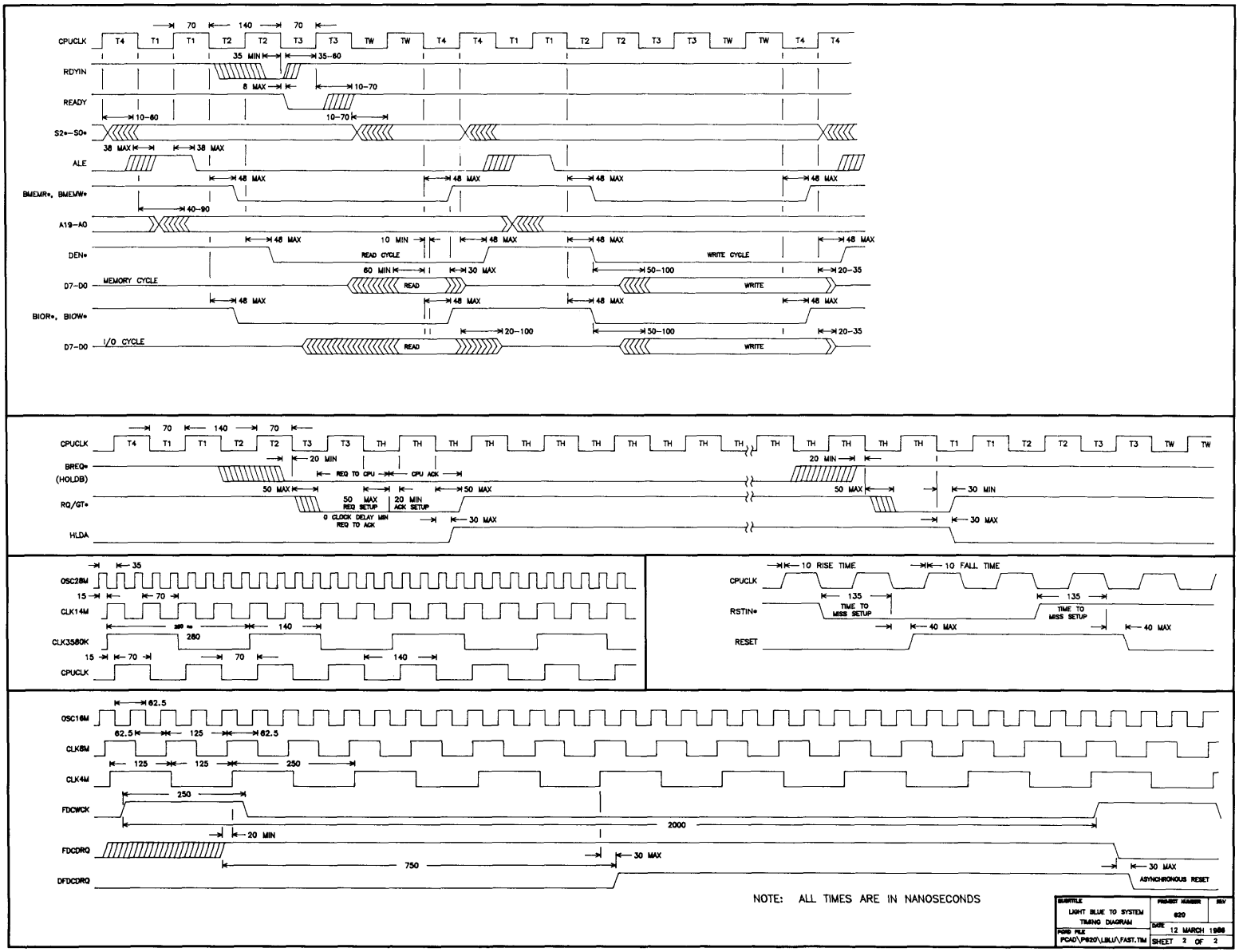


Figure 2 (Cont.) Light Blue to System Timing (2 of 2)

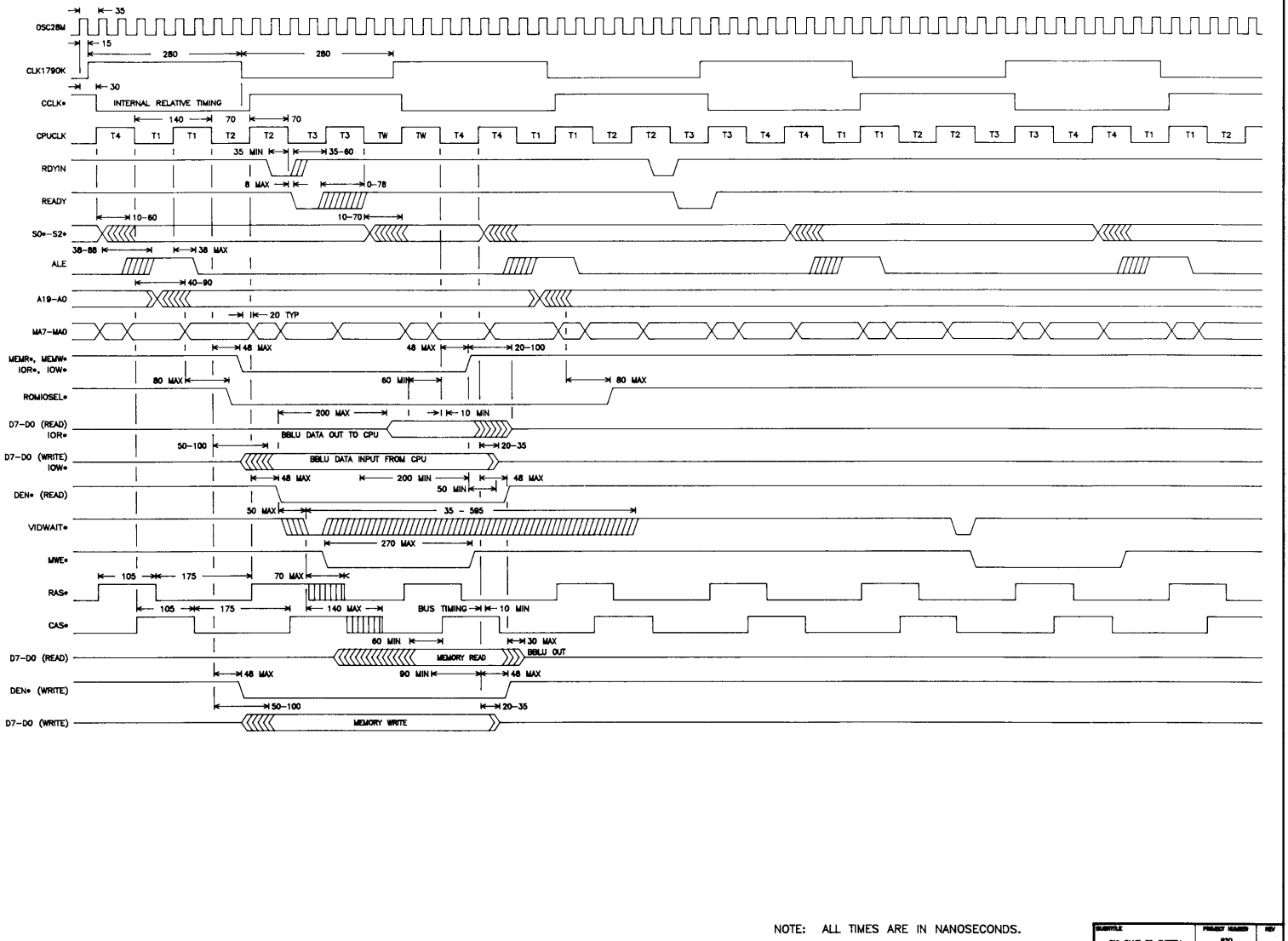


Figure 3. Big Blue to System Timing (1 of 2)

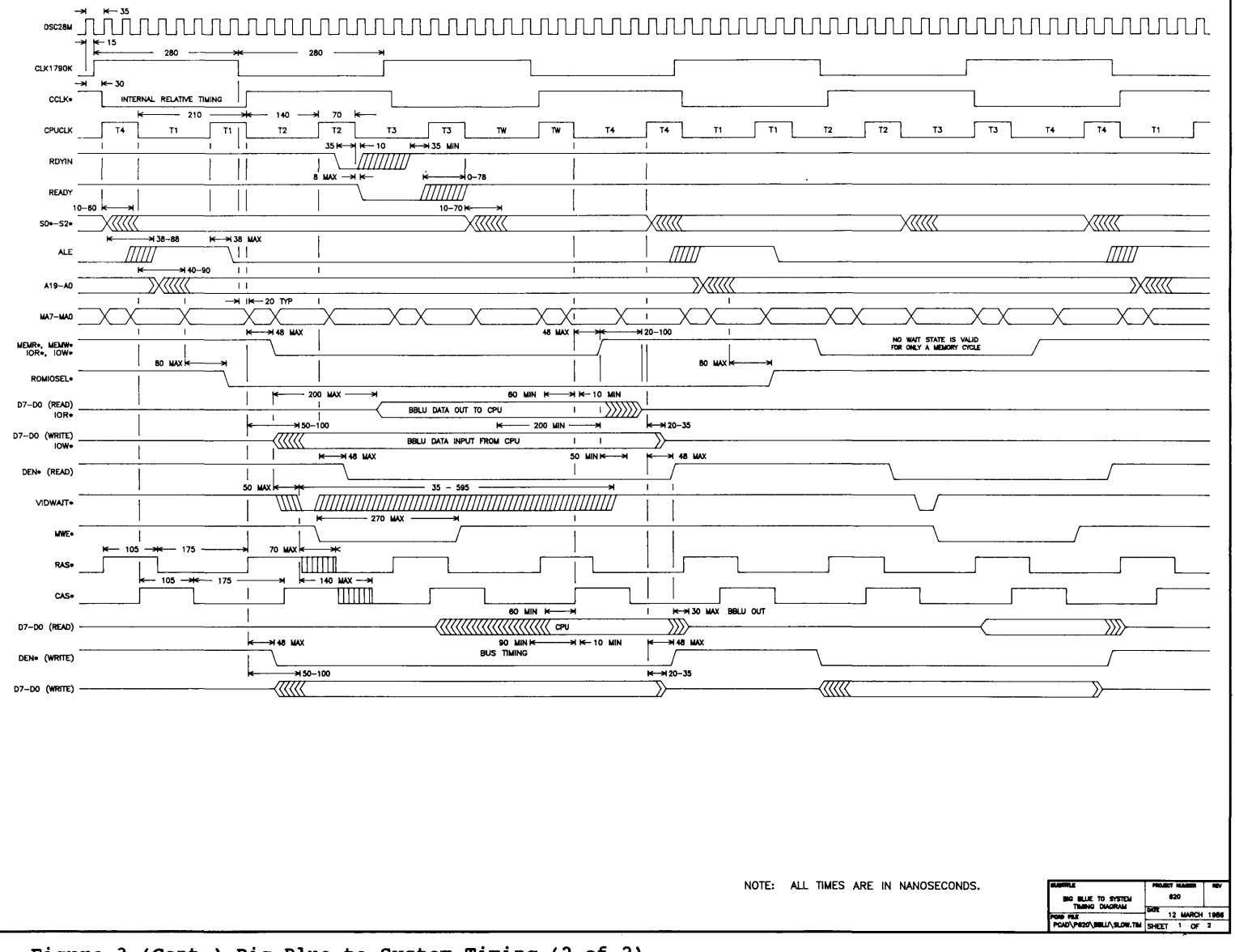


Figure 3 (Cont.) Big Blue to System Timing (2 of 2)

THEORY OF OPERATION

Main Logic Board

The Block Diagram of the main logic board (Figure 4) shows the basic functional divisions.

CPU Function

The CPU function consists of the CPU (Intel 8088), the address, data interface, the CPU control signal generator, the bus control signal generator and the interrupt controller (Intel 8259A). It is located near the DC Power connector.

Non-CPU Function, Main Logic Board

The non-CPU functions can be divided into two main parts: memory and I/O. Memory consists of RAM and ROM. RAM or Video/System Memory (Figure 5) serves as storage for both the video data and program data. ROM memory contains the BIOS and diagnostics. I/O consists of all the peripheral functions; keyboard, floppy disk controller, printer, joystick and sound.

Processor Address/Data Interface

The 8088 has three groups of Address/Data lines; AD0 - AD7, A8 - A15 and A16 - A19. AD0 - AD7 are multiplexed address and data lines. To separate and save the address that comes out first, the signals are applied to U20 (74HCT373) and latched by ALE. Additionally, the signals are applied to data transceiver U13 (74HCT245). U13 is enabled only during the data portion of the CPU cycle. (The exception is during an Interrupt Acknowledge cycle.) Direction of transmission is controlled by the RD* (READ) signal from the Timing Control Generator. Address lines A8 - A15 are present during the entire CPU cycle and need only to be buffered. Address lines A16 - A19 are multiplexed with status signals S4 - S7 and need to be latched. The results are: A8 - A11, A16 - A19 are latched into U19 (74HCT373) by ALE and A12 - A15 are buffered by half of U18 (74HCT244). The outputs from these latches/buffers/transceivers are the BUS Signals A00 - A19, D0 - D7.

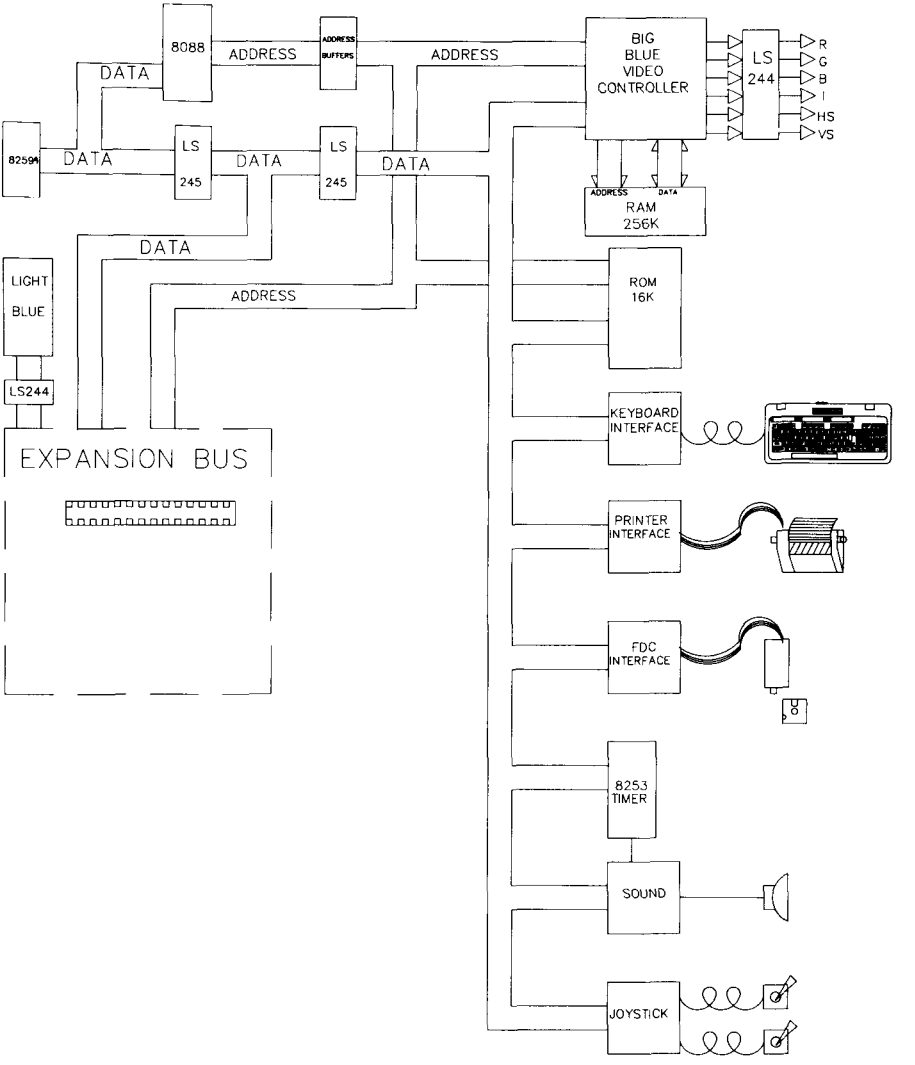


Figure 4. Main Logic Block Diagram

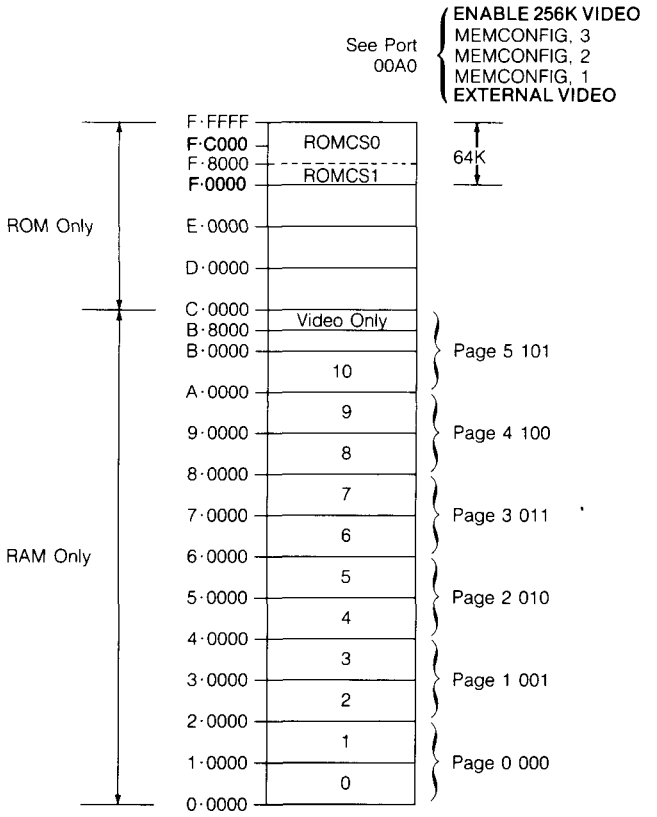


Figure 5. Memory Map

CPU Control Signal Generation

The 8088 CPU uses a 4.77 (7.16) MHz clock with a special duty cycle (33% (4.77) high, 67% low) (7.16 -> 50% High 50% Low). This clock is produced by the Timing Control Generator. The Timing Control Generator receives a 28 MHz input clock and divides it by 6 to produce 4.77 MHz CPUCLK or by 4 to produce 7.16 MHz CPUCLK and by 24 to produce D4CLK (1.193 MHz). In addition to being used by the control signal logic, the clocks are buffered by U18 (74HCT244) for the bus signals OSCY (14 MHz), CLKY (CPU clock) (4.77/7.16 MHz). (See the Bus Interface Specification).

The RESET signals (RESET, BRESET, RST*) originate at U16 (Timing Control Generator) which synchronizes the input RES*. RES* originates from C130 which is shorted to 0 volts by diode CR2 when the power is off.

The READY circuit synchronizes the system "ready" signals with the CPU clock and generates the CPU input READY. If a function needs one or more "wait" states added to its access, it must set the RDYIN line low. From the main logic board, RDYIN is set low by the sound IC for 32 extra "wait states" and the video/system memory sets RDYIN low for typically one or two "wait" cycles. The READY circuit of the Timing Control Generator (U16) is operated in the non-asynchronous mode; i.e. two sequential edges of clock (a rising edge first) are required to set the READY signal true. RDYIN is pulled-up by R30.

IFL Equations

U3 Buffer Control **Checksum: 50C9**

Inputs		Outputs
PIN 1 = !mio	PIN 7 = !fdcack	PIN 14 = iomb
PIN 2 = !memr	PIN 8 = !ior	Pin 15 = enbnmi
PIN 3 = al9	PIN 9 = !refresh	PIN 16 = !romcs
PIN 4 = al8	PIN 11 = nmien	PIN 17 = !bufenb
PIN 5 = al7	PIN 12 = nmi	PIN 18 = bufdir
PIN 6 = !memios	PIN 13 = al6	PIN 19 = !bbrfsh

Equations:

```
/**  Logic Equations **/
bbrfsh = refresh;
!bufdir = memr & !mio & !fdcack
          #memr & !mio & memios
          #memr & !mio & ior
          #ior & mio
          #ior & fdcack & !memios &!memr;
!bufenb = !memios & !romcs & !fdcack
          #memios & fdcack;
romcs = memr & !refresh & al9 & al8 & al7 & al6;
iomb = !mio;
enbnmi = nmien & nmi;
```

System Control Signal Generation

The Timing Control Generator (U16) provides the timing strobes required by the system. These include IOW*, IOR*, MEMW*, MEMR*, ALE, DEN* and IO/M*. These signals are synthesized 8088 status signals S0*, S1*, S2* and INTCS* (8258A chip select). See Figure 6.

All external devices, except the 8259A Interrupt Controller, are buffered by an LS244 that is controlled by the DEN* signal. Since the 8259A is not buffered, the DEN* signal must remain inactive during accesses to the 8259A.

Bus Specification

Specifications for the bus will include the expansion connector pin/signal assignments and the signal characteristics. Refer to the Expansion I/F Connector diagram. See Figure 7.

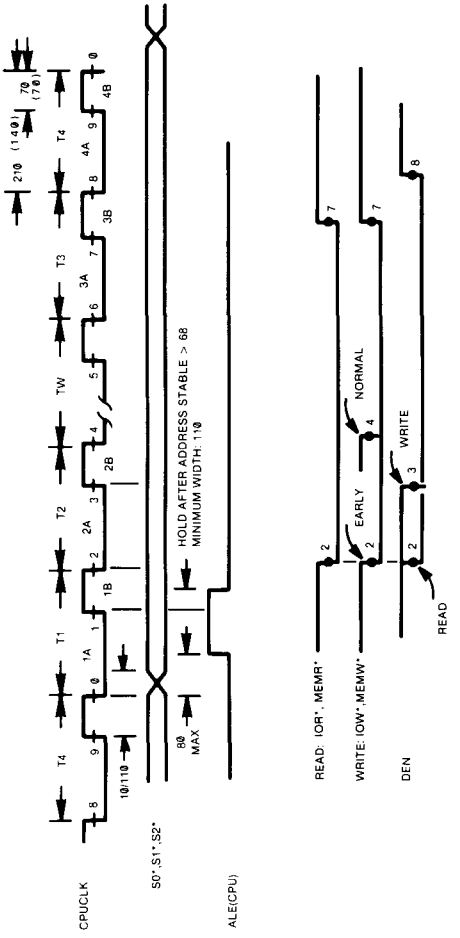


Figure 6. System Control Timing

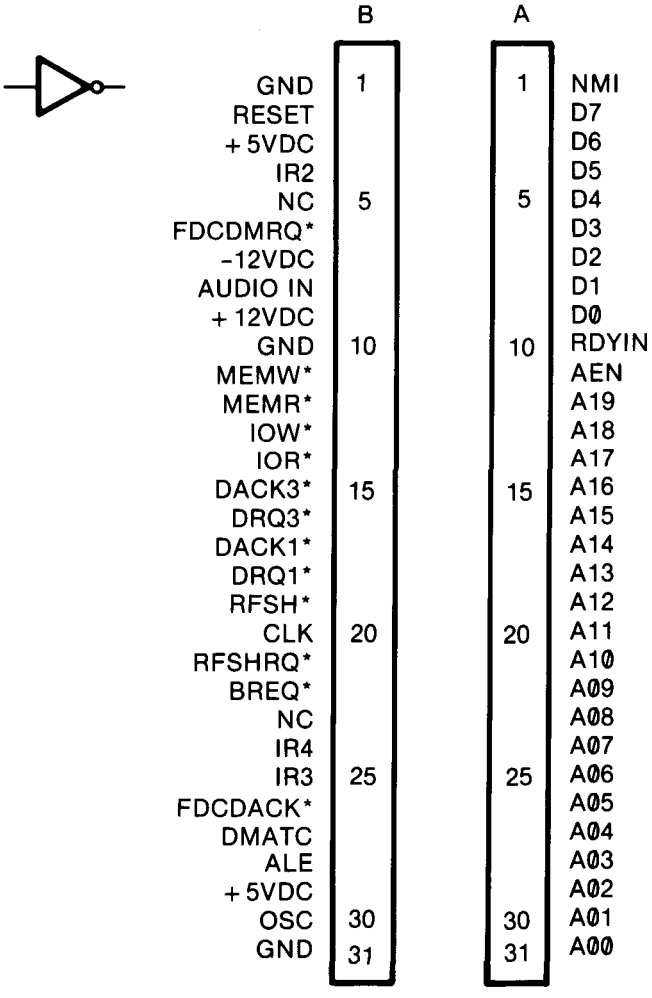


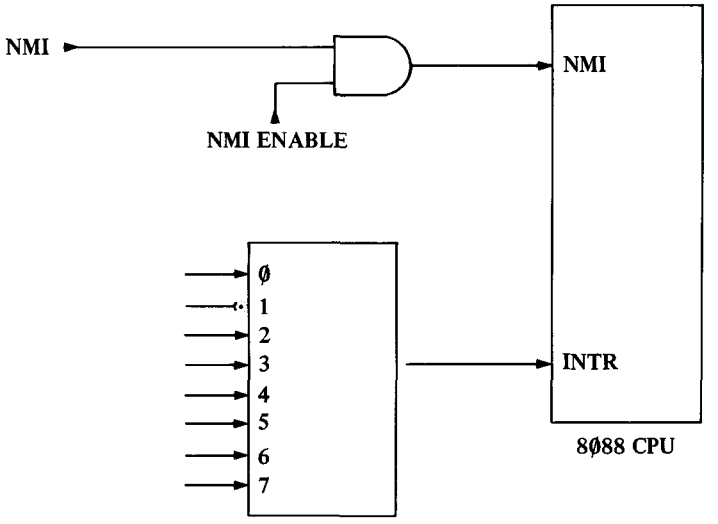
Figure 7. Expansion I/F Connector

Interrupt Function

The 8088 supports two types of interrupts: maskable (by the CPU, INT) and non-maskable (NMI). See Figure 8. The 8259A Interrupt Controller is the source of the INT for the 8088. The 8259A has eight interrupt inputs controlled through software commands. It can mask (disable) and prioritize (arrange priority) to generate INT. These eight interrupts are:

#0	Timer Channel 0	Software Timer
#1	Keyboard	Keyboard Code Received
#2	Hard Disk Controller	Optional Function, Interrupt on Bus
#3	Comm 2	Optional Function, Interrupt on Bus
#4	Comm 1	Optional Function, Interrupt on Bus
#5	Vertical Sync	Software Timer for Video
#6	Disk Controller, Floppy	Ready to Receive/Transmit Data
#7	Printer	Data Transmission Complete

The NMI interrupt is not maskable by the CPU but it can be enabled/disabled by hardware. The enable is at Port 00A0 Bit 7. The enable is cleared by RESET. There is no specific function assigned to NMI and it is available on the bus.



8259A INTERRUPT CONTROLLER

INTERRUPT	FUNCTION
NMI	AVAILABLE ON BUS
Ø	8253 TIMER CH Ø (REFRESH)
1	KEYBOARD
2	HARD DISK
3	SECONDARY COMM.
4	PRIMARY COMM.
5	VERTICAL SYNC.
6	FLOPPY DISK CONTROLLER
7	PARALLEL PORT

Figure 8. Interrupt Structure

Bus Interface

The interface to the main bus is divided into three parts: address/control strobes, memory data and I/O data. The address/control strobe part (BA0 - BA19, BMEMR*, BMEMW*, BIOR*, BIOW*) is shared by both the I/O and the memory sections. Input buffers are U18, U20 and U19. One function of the address bus is the select logic for each of the functions. U24 decodes all the I/O chip selects except those for the Video/System Memory I/O ports which are decoded by U28. The memory selects are decoded by U28. The I/O data transceiver is U11 with its output enable and direction control decoded by U3.

Keyboard / Timer / Sound Circuits

Included in the Array is an 8255 programmable peripheral interface equivalent design. It has three 8 bit parallel ports, A, B and C. Port A is configured as an input port and is used for keyboard data. Port B is configured as an output port and is used for control signals for the sound, keyboard and timer functions. Port C is split into 4 inputs, including the timer channel and #2 monitor and 4 outputs including the keyboard/multifunction interface signals.

Keyboard Interface

The Keyboard Interface consists of an 8048 (U6) CPU and a Keyboard (U10) Controller. The 8048 generates strobes to the keyboard. Data from the keyboard is received by the 8048, translated to an 8 bit asynchronous serial format, and transmitted to the Keyboard Controller. The Keyboard Controller translates this serial data into a parallel format and makes it available to the data bus. The serial data from the 8048 consists of a clock signal and a data signal. The clock consists of 8 consecutive positive pulses (signal normal state is logic low). The rising edge of each pulse is centered in the middle of each data period. The data signals consists of 8 data periods and an "end-of-character" bit. Normal state of the data signal is logic high which represents a logic 1. Thus, the data signal will change only if the data bit is a 0. The ninth and last data bit is always a 0. In the absence of a ninth clock, it will set the interrupt and busy signals. See Figure 9 for the Keyboard Timing Chart.

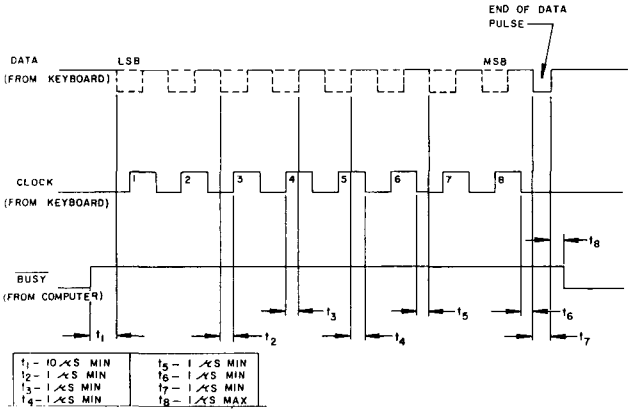


Figure 9. Keyboard Timing Chart

Timer Function

The Timer is an 8253 Timer/Counter consisting of three independent counters. The clock for all three counters is 1.1925 MHz. The gate for counter #0, #1 is permanently "on". The gate for counter #2 is controlled by a bit of the keyboard interface (8255 Port B). The output of counter #0 is dedicated to system interrupt #0 (8259 IR0) for software timing functions. The output of counter #1 is dedicated to the REFRESH function. When the optional DMA/Memory board is installed, DMA channel #0 is used for refreshing the RAM memory. Counter #1 sets RFSHRQ* (DRQ0) every 15 micro-seconds to initiate a single "dummy" memory read. The output of counter #2 is routed to the sound circuit and into the 8255 Port C for monitoring by the CPU. See Figure 10.

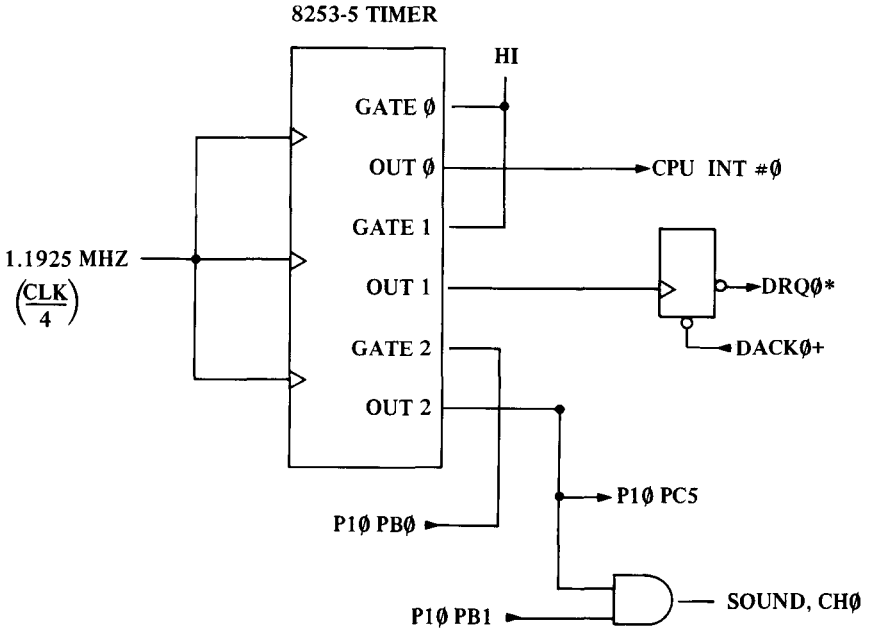
Sound Function

The sound function consists of an internal and an external sound circuit. These are directly connected to the speaker via U4. The source of the sound frequencies is U15 Complex Sound Generator. Internally, U15 has four programmable sound generators. The frequency and output level of each is controlled by software. The four internal generators are summed with an external input into a single output. The external source is from the 8253 counter #2 (programmable frequency and fixed amplitude). It is one of three selectable sources for the external audio out signal. This signal is intended as an input into an external earplug. The two sound frequency sources are:

1. Complex sound generator U15.

2. The 8253 counter at channel 2.

These are selected by an analog multiplexer U1. Selection signals are SNDCNTL0, SNDCNTL1 from the keyboard interface. The output driver for Audio Out is U4 which is designed to drive a load impedance of 1000 ohms. See Figure 11.



CHANNEL Ø: MODE Ø, INTERRUPT ON T/C
1: MODE Ø, NEGATIVE PULSE ON T/C
2: MODE 3, SQUARE WAVE OUTPUT

Figure 10. System Timer 8253-5

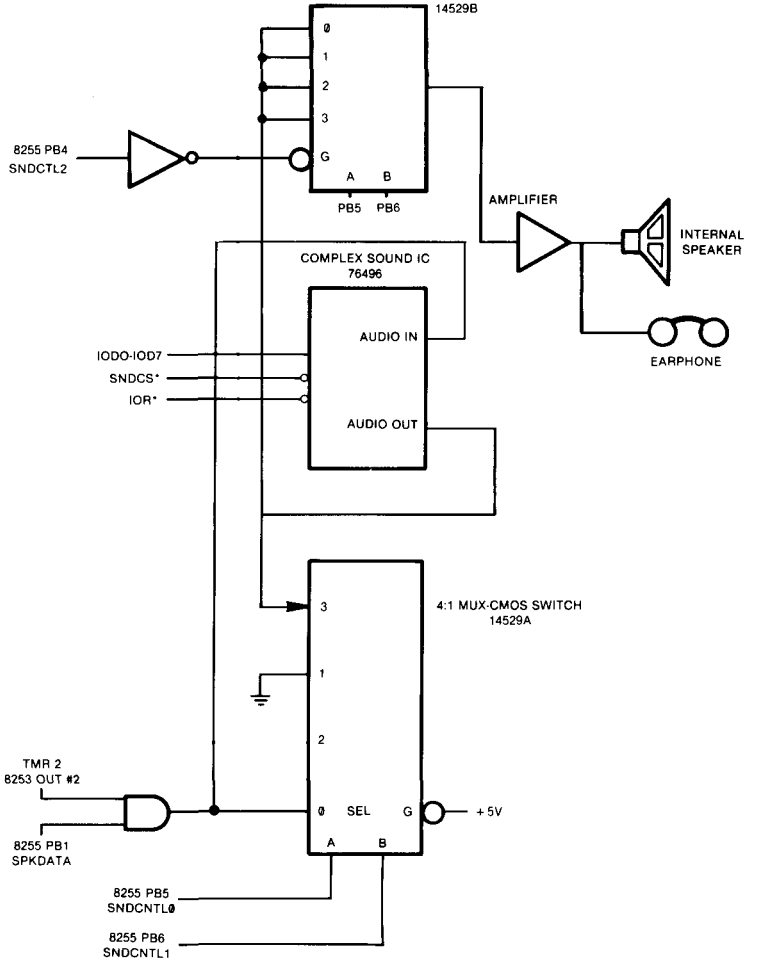


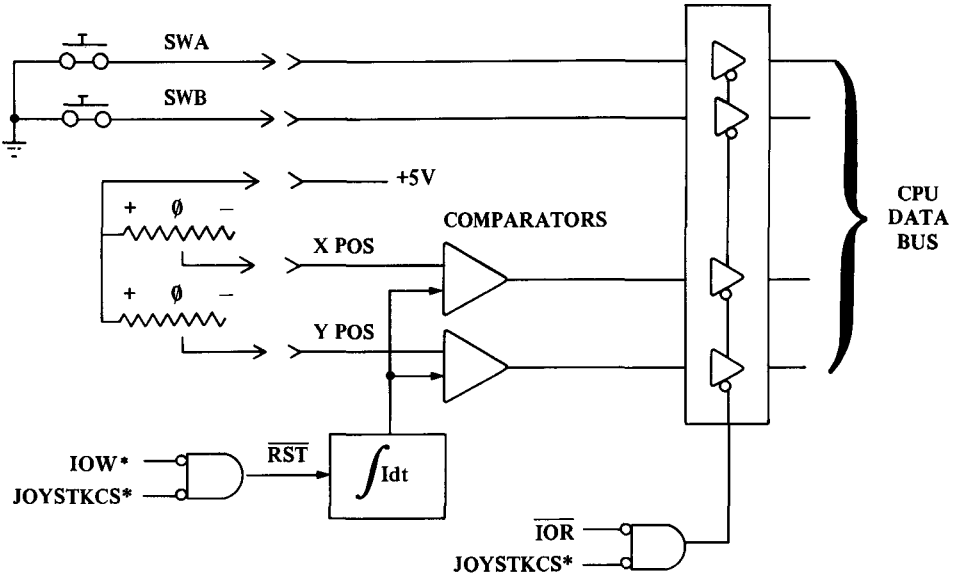
Figure 11. Sound Functional Block Diagram

Joystick Interface

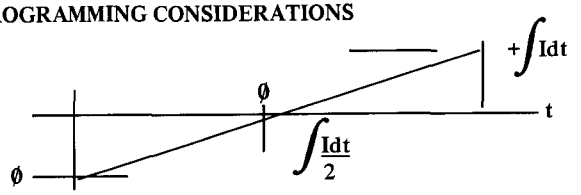
The joystick interface converts positional information from hand-held joysticks (1 or 2) into CPU data. Each joystick provides 1 or 2 push-buttons and X, Y position for a total of 4 bits each. You can use 2 joysticks. The joystick handle is connected to two potentiometers mounted perpendicular to each other; one for X position, one for Y position. Through the cable, the main logic board applies +5 VDC to one side and ground to the other of the pots. The pot wiper is the position signal: a voltage between 0 and +5 VDC. This signal is applied to one input of a comparator U21. The other comparator input is the reference signal (a ramp between 0.0 to +5.0 volts.) When the position signal is equal or less than the reference signal, the comparator output goes true. This comparator output is the X or Y position data bit. The ramp is reset to 0.0 VDC whenever a "write" is made at Port 200/201 Hex. The IOW* signal turns on Q2, which drains C127 to 0.0 volts. When Q2 is turned off, Q1, R22, R27, R39, and CR3 create a constant-current source that linearly charges C127 to +5.0 VDC in 1.12 milliseconds. The joystick information is "read" by the CPU at Port 200/201 Hex through U23. See Figure 12.

Printer Interface

The printer interface is totally contained in a custom Gate Array U32 and is shown in Figure 13. Functionally, the printer interface consists of an output data latch (write @ 378) and accompanying input data buffer. The latch and buffer reads back the output data (read @ 37A) with an accompanying input buffer for read-back (read @ 37A). The input buffer is for reading printer input signals (read @ 379), I/O address decoding, data transceiver, and interrupt logic. The interrupt is (logically) ACKNOWLEDGE* if interrupts are enabled (37A Bit 4).



PROGRAMMING CONSIDERATIONS



IOR's
@ REGULAR INTERVALS

ONCE TRIGGERED BY SOFTWARE THE INTERGRATOR CIRCUIT PRODUCES A PULSE THE DURATION OF WHICH IS DEPENDENT ON JOYSK POSITION.

Figure 12. Joystick I/F

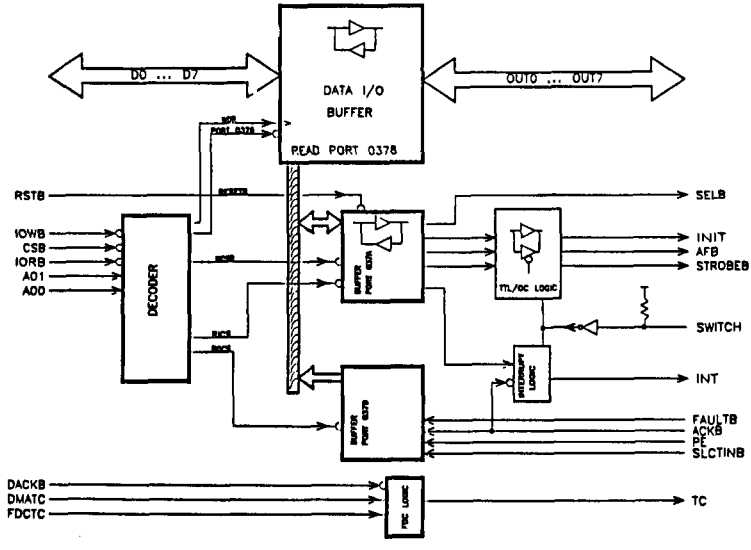


Figure 13. Printer Block Diagram

Floppy Disk Controller Interface

The Floppy Disk Controller interface consists of the 765 controller and support circuitry. The clocks are generated by the Timing Control Generator. The 4.00 MHz (FDCCLK) signal is applied to the FDC for its internal processor clock (CLK pin 19). FDC WCK is a 250 nanosecond pulse every 2.0 microseconds. The descriptions of several of the control signals are discussed in the Timing Control Generator. Counter U26 is used to add pre-compensation to the MFM coded write data (250 nanosecond pulse every 2.0 microseconds maximum). The 765 FDC signals "early" and "late" determine the number of 8 MHz clock periods (125 nanoseconds) the write data is delayed thru U29 - normal = 6, early = 4, late = 7. Data separator U29 converts "raw data" from the drive into read data (RDD) and read clock (RDW).

Video System Logic

A major block of the Tandy 1000 EX is the video interface circuitry. A block diagram of the video controller circuit is shown in Figure 14. This custom part contains all of the logic necessary to generate an IBM compatible color video display. The video interface logic consists of the 84 pin custom video circuit, 8 - 64K X 4 RAMs, a 74LS244 buffer, and associated logic for generation of composite video.

The Tandy 1000 EX video interface circuitry controls 256K of memory. See Video System Memory Map, Figure 15. This RAM is shared by the CPU and the video. Normally, the video only requires 16K or 32K for the video screen and the remainder of the 256K is available for system memory uses.

The Tandy 1000 EX video interface custom circuit is composed of a 6845 equivalent design, dynamic RAM address generation/ timing (see Figure 16.), and video attribute controller logic.

Normal functioning of the video interface custom circuit is as follows: After the 6845 is programmed with a correct set of operating values (see Table 1), the address inputs to the dynamic RAMs are generated by a 4:1 multiplexer. This MUX switches between video (6845) addresses and CPU addresses as well as between row and column addresses. In addition, the video interface chip provides the RAM timing signals and generates a wait signal to CPU for proper synchronization with the video RAM access cycles.

The outputs from the RAM chips are only connected to the video interface custom circuit, so all CPU read/write operations are buffered by this part. During a normal display cycle, video data from the RAM chips is first latched in the Video Attribute latch and the Video Character latch. The video interface requires a memory organization of 64K X 16 and will latch 16 bits of memory during each access to RAM. From the output of the two latches, the data is supplied to the character ROM for the Alpha modes or to the shift registers for graphics modes. A final 2:1 MUX is used to switch between foreground or background in the alpha mode.

From the 2:1 MUX, the RGBI data is combined with the PC color select data and latched in the Pre-Palette latch. This latch synchronizes the RGBI data before it is used to address the palette.

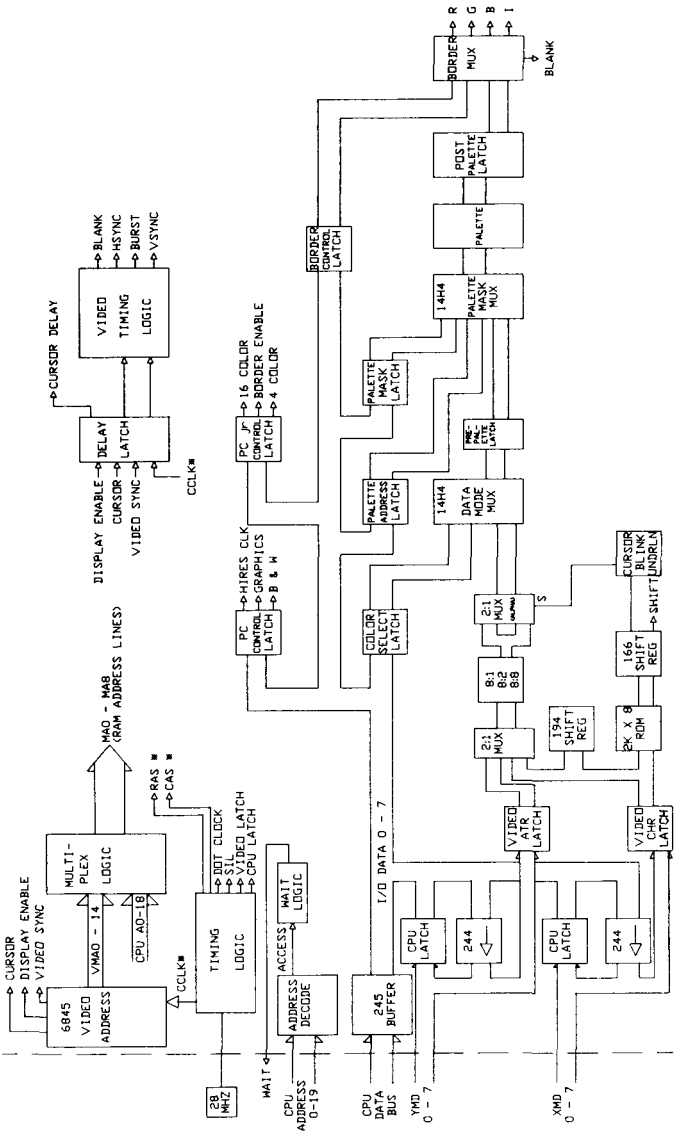


Figure 14. Video Controller Block Diagram

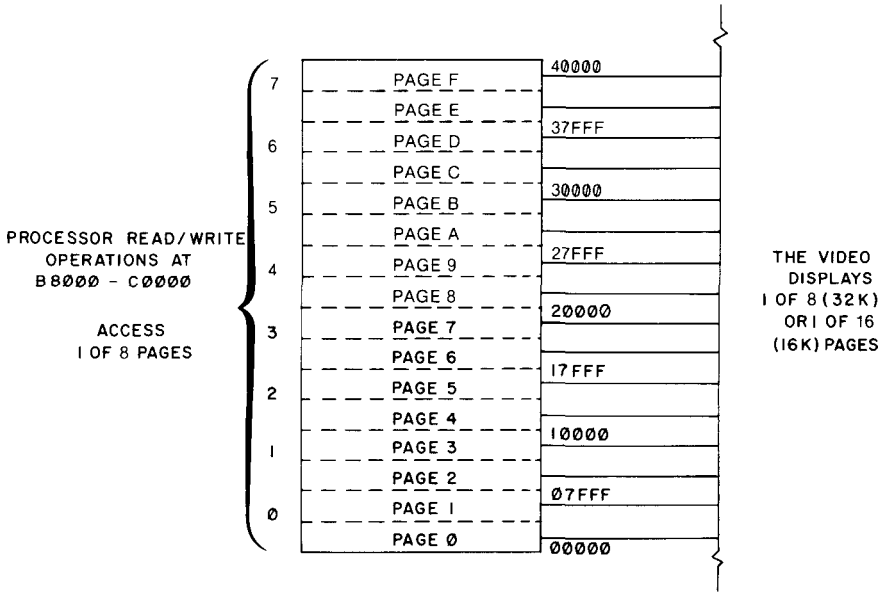


Figure 15. Video System Memory Map

Main System Board Ram Timing Specification

AC Operating Conditions and Characteristics

Parameter	Symbol	Min.	Max.	Units
Random Read or Write Cycle Time	tRC	279	--	ns
Read Write Cycle Time	tRWC	279	--	ns
Access Time from Row Address Strobe	tRAC	--	200	ns
Access Time from Column Address	tCAC	--	100	ns
Output Buffer and Turn-Off Delay	tOFF	0	30	ns
Row Address Strobe Precharge Time	tRP	100	--	ns
Row Address Strobe Pulse Width	tRAS1	170	--	ns
Column Address Strobe Pulse Width	tCAS	130	--	ns
Row Address Setup Time	tASR	0	--	ns
Row Address Hold Time	tRAH	20	--	ns
Column Address Setup Time	tASC	0	--	ns
Column Address Hold Time	tCAH	35	--	ns
Transition Time (Rise and Fall)	tT	--	50	ns
Read Command Setup Time	tRCS	0	--	ns
Read Command Hold Time	tRCH	0	--	ns
Read Command Hold Time Referenced to RAS	tRRH	0	--	ns
Write Command Hold Time	tWCH	35	--	ns
Write Command Hold Time Referenced to RAS	tWCR	95	--	ns
Write Command Pulse Width	tWP	35	--	ns
Write Command to Row Strobe Lead Time	tRWL	45	--	ns
Write Command to Column Strobe Lead Time	tCWL	45	--	ns
Data in Setup Time	tDS	0		ns
Data in Hold Time	tDH	35	--	ns
Data in Hold Time Referenced to RAS	tDHR	95	--	ns
Column to Row Strobe Precharge Time	tCRP	0	--	ns
RAS Hold Time	tRSH	85	--	ns
Refresh Period	tRFSH	--	2.0	ns
WRITE Command Setup Time	tWCS	0	--	ns
CAS to WRITE Delay	tCWD	45	--	ns
RAS to WRITE Delay	tRWD	120	--	ns
CAS Hold Time	tCSH	200	--	ns

Figure 16. Main System Board RAM Timing Specification

PROGRAMMING TABLE FOR THE 6845 All Values in Hex (Decimal)

Register Address	40 x 25 Alpha	80 x 25 Alpha	Low Res. Graphics	High Res. Graphics	40 x 25 Alpha	80 x 25 Alpha	Low Res Graphics	High Res Graphics
	Monitor Mode				**TV Mode**			
00 Horizontal Total	38 (56)	71 (113)	38 (56)	71 (113)	38 (56)	71 (113)	38 (56)	71 (113)
01 Horizontal Displayed	28 (40)	50 (80)	28 (40)	50 (80)	28 (40)	50 (80)	28 (40)	50 (80)
02 Horizontal Sync Position	2D (45)	59 (89)	2D (45)	59 (89)	2D (45)	59 (89)	2D (45)	59 (89)
03 Horizontal Sync Width	08 (8)	10 (16)	08 (8)	10 (16)	08 (8)	10 (16)	08 (8)	10 (16)
04 Vertical Total	1C (28)	1C (28)	7F (127)	3F (63)	1F (31)	1F (31)	7F (127)	3F (63)
05 Vertical Total Adjust	01 (1)	01 (1)	06 (6)	06 (6)	06 (6)	06 (6)	06 (6)	06 (6)
06 Vertical Displayed	19 (25)	19 (25)	64 (100)	32 (50)	19 (25)	19 (25)	64 (100)	32 (50)
07 Vertical Sync Position	1A (26)	1A (26)	70 (112)	38 (56)	1C (28)	1C (28)	70 (112)	38 (56)
08 Interlace Mode	02 (2)	02 (2)	02 (2)	02 (2)	02 (2)	02 (2)	02 (2)	02 (2)
09 Max Scan Line Address	08 (8)	08 (8)	01 (1)	03 (3)	07 (7)	07 (7)	01 (1)	03 (3)
10 Cursor Start	06 (6)	06 (6)	06 (6)	06 (6)	06 (6)	06 (6)	06 (6)	06 (6)
11 Cursor End	07 (7)	07 (7)	07 (7)	07 (7)	07 (7)	07 (7)	07 (7)	07 (7)
12 Start Address (High)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)
13 Start Address (Low)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)

Table 1

The palette mask MUX is used to switch between incoming RGBI data and the palette address register. During a CPU write to the palette, this address register selects one of the 16 palette locations. Also, the palette mask MUX allows any of the input RGBI bits to be set to zero.

The palette allows the 16 colors to be remapped in any desired organization. Normally the pallete is set for a 1:1 mapping (red = red, blue = blue, etc.) for PC compatibility. However, instantly changing the on-screen colors is a very powerful tool for animation or graphics programs.

After the palette, the RGBI data is resynchronized in the Post Palette register. The final logic before the RGBI data is buffered off the chip is the Border MUX. This MUX allows the Border to be replaced with any color selected by the border color latch. This latch is normally disabled in PC modes, but it is used in all PCjr modes.

I/O MAP SUMMARY

Block	Usage	Function
0000-001F	0000-000F	DMA Function
0020-003F	0020-0021	Interrupt Controller
0040-005F	0040-0043	Timer
0060-007F	0060-0063	PIO Function
0080-009F	0080-0083	DMA Page Register
00A0-00BF	00A0	NMI Mask Register
00C0-00DF	00C0-00C1	Sound Generator
00E0-01FF		Reserved
0200-020F	0200-0201	Joystick Interface
0210-031F		Reserved
0320-032F		Reserved Hard Disk
0330-036F		Not Assigned
0370-037F	0378-037B	Printer
0380-03CF		Not Used
03D0-03DF	All	System Video
03E0-03EF		Reserved
03F0-03FF	03F2,F4,F5	Floppy Disk Controller
0400-FFFF		Not Usable

Address	Description
0000	DMA Controller IOW* = 0: Channel 0 Base and Current Address Internal Flip/Flop = 0: Write A0-A7 Internal Flip/Flop = 1: Write A8-A15 IOR* = 0: Channel 0 Current Address Internal Flip/Flop = 0: Read A0-A7 Internal Flip/Flop = 1: Read A8-A15
0001	DMA Controller IOW* = 0: Channel 0 Base and Current Word Count Internal Flip/Flop = 0: Write W0-W7 Internal Flip/Flop = 1: Write W8-W15 IOR* = 0: Channel 0 Current Word Count Internal Flip/Flop = 0: Read W0-W7 Internal Flip/Flop = 1: Read W8-W15
0002	DMA Controller IOW* = 0: Channel 1 Base and Current Address Internal Flip/Flop = 0: Write A0-A7 Internal Flip/Flop = 1: Write A8-A15 IOR* = 0: Channel 1 Current Address Internal Flip/Flop = 0: Read A0-A7 Internal Flip/Flop = 1: Read A8-A15

Address	Description
0003	DMA Controller IOW* = 0: Channel 1 Base and Current Word Count Internal Flip/Flop = 0: Write W0-W7 Internal Flip/Flop = 1: Write A8-A15 IOR* = 0: Channel 1 Current Word Count Internal Flip/Flop = 0: Read W0-W7 Internal Flip/Flop = 1: Read W8-W15
0004	DMA Controller IOW* = 0: Channel 2 Base and Current Address Internal Flip/Flop = 0: Write A0-A7 Internal Flip/Flop = 1: Write A8-A15 IOR* = 0: Channel 2 Current Address Internal Flip/Flop = 0: Read A0-A7 Internal Flip/Flop = 1: Read A8-A15
0005	DMA Controller IOW* = 0: Channel 2 Base and Current Word Count Internal Flip/Flop = 0: Write W0-W7 Internal Flip/Flop = 1: Write W8-W15 IOR* = 0: Channel 2 Current Word Count Internal Flip/Flop = 0: Read W0-W7 Internal Flip/Flop = 1: Read W8-W15
0006	DMA Controller IOW* = 0: Channel 3 Base and Current Address Internal Flip/Flop = 0: Write A0-A7 Internal Flip/Flop = 1: Write A8-A15 IOR* = 0: Channel 3 Current Address Internal Flip/Flop = 0: Read A0-A7 Internal Flip/Flop = 1: Read A8-A15
0007	DMA Controller IOW* = 0: Channel 3 Base and Current Word Count Internal Flip/Flop = 0: Write W0-W7 Internal Flip/Flop = 1: Write W8-W15 IOR* = 0: Channel 3 Current Word Count Internal Flip/Flop = 0: Read W0-W7 Internal Flip/Flop = 1: Read W8-W15

0008 DMA Controller
IOW* = 0, Write Command Register

Bit	Description
0	0 = Memory to Memory Disable 1 = Memory to Memory Enable
1	0 = Channel 0 Address Hold Disable 1 = Channel 0 Address Hold Enable X If bit 0 = 0
2	0 = Controller enable 1 = Controller disable
3	0 = Normal timing 1 = Compressed timing X If bit 0 = 1
4	0 = Fixed priority 1 = Rotating priority
5	0 = Late write selection 1 = Extended write selection X = If bit 3 = 1
6	0 = DREQ sense active high 1 = DREQ sense active low
7	0 = DACK sense active low 1 = DACK sense active high

IOR* = 0, Read Status Register

Bit	Description
0	1 = Channel 0 has reached TC
1	1 = Channel 1 has reached TC
2	1 = Channel 2 has reached TC
3	1 = Channel 3 has reached TC
4	1 = Channel 0 Request
5	1 = Channel 1 Request
6	1 = Channel 2 Request
7	1 = Channel 3 Request

0009 DMA Controller
IOW* = 0, Write Request Register

Bit	Description		
0-1	Bit1	Bit0	
	0	0	Select channel 0
	0	1	Select channel 1
	1	0	Select channel 2
	1	1	Select channel 3
2	0	Reset request bit	
	1	Set request bit	
3-7	Don't Care		

IOR* = 0, Illegal

000A DMA Controller
IOW* = 0, Write Single Mask Register

Bit	Description		
0-1	Bit1	Bit0	
	0	0	Select channel 0 mask bit
	0	1	Select channel 1 mask bit
	1	0	Select channel 2 mask bit
	1	1	Select channel 3 mask bit
2	0	Clear mask bit (Disable Channel)	
	1	Set mask bit (Disable Channel)	
3-7	Don't care		
	IOR* = 0, Illegal		

000B DMA Controller
IOW* = 0, Write Mode Register

Bit	Description		
0-1	Bit1	Bit0	
	0	0	Channel 0 select
	0	1	Channel 1 select
	1	0	Channel 2 select
	1	1	Channel 3 select
2-3	Bit3	Bit2	
	0	0	Verify transfer
	0	1	Write transfer to memory
	1	0	Read transfer to memory
	1	1	Illegal
	X	If bits 6 and 7 = 11	
4	0	Autoinitialization disable	
	1	Autoinitialization enable	
5	0	Address increment select	
	1	Address decrement select	
6-7	Bit7	Bit6	
	0	0	Demand mode select
	0	1	Single mode select
	1	0	Block mode select
	1	1	Cascade mode select
	IOR* = 0, Illegal		

000C DMA Controller
IOW* = 0, Clear Byte Pointer Flip/Flop
IOR* = 0, Illegal

000D	DMA Controller IOW* = 0, Master Clear IOR* = 0, Read Temporary Register
000E	DMA Controller IOW* = 0, Clear Mask Register IOR* = 0, Illegal
000F	DMA Controller IOW* = 0, Write all Mask Register Bits

Bit	Description
0	0 = Clear channel 0 mask bit (Enable) 1 = Set channel 0 mask bit (Disable)
1	0 = Clear channel 1 mask bit (Enable) 1 = Set channel 1 mask bit (Disable)
2	0 = Clear channel 2 mask bit (Enable) 1 = Set channel 2 mask bit (Disable)
3	0 = Clear channel 3 mask bit (Enable) 1 = Set channel 3 mask bit (Disable)
4-7	Don't care IOR* = Illegal

0010 - 001F	Not Used

Address	Description
0020	8259A Interrupt Controller

Note: Initialization Words are setup by the operating system and are generally not to be changed. Writing an initialization word may cancel pending interrupts.

Bit4 = 1: INITIALIZATION COMMAND WORD 1

```
Bit0 = 0:  ICW4 needed
     = 1:  ICW4 not needed
Bit1 = 0:  Cascade Mode
     = 1:  Single
Bit2 = Not used
Bit3 = 0:  Edge Triggered Mode
     = 1:  Level Triggered Mode
           when the SL bit is active
Bit5 - 7:  Not Used
```

```
Bit4 = 0 &          OPERATION CONTROL WORD 2
Bit3 = 0            Bit0 - 2:  Determine the interrupt level acted on
                               when the SL bit is active

                               Interrupt Level = 0 1 2 3 4 5 6 7
                                    Bit0 (L0):   0 1 0 1 0 1 0 1
                                    Bit1 (L1):   0 0 1 1 0 0 1 1
                                    Bit2 (L2):   0 0 0 0 1 1 1 1

                    Bit5 - 7   Control Rotate and End of Interrupt
                                modes

B7 B6 B5
 0  0  1   Non-specific EOI command                  End of Interrupt
 0  1  1   Specific EOI command                      End of Interest
 1  0  1   Rotate on non-specific EOI command       Automatic Rotation
 1  0  0   Rotate in Automatic EOI Mode (set)       Automatic Rotation
 0  0  0   Rotate in Automatic EOI Mode (clear)     Automatic Rotation
 1  1  1   *Rotate on Specific EOI command         Specific Rotation
 1  1  0   *Set priority command                    Specific Rotation
 0  1  0   No operation

  *L0 - L2 are used

Bit4 = 0 &          OPERATION CONTROL WORD 3
Bit3 = 1            Bit0 - 1:
                    Bit1 Bit0- Read Register Command
                      0    0 - No Action
                      0    1 - No Action
                      1    0 - Read IR Register on next IOR* Pulse
                      1    1 - Read IS Register on next IOR* Pulse

                    Bit2 = 0:  No Poll Command
                         = 1:  Poll Command

                    Bit5 - 6:

                    Bit6 Bit5- Special Mask Mode
                      0    0 - No Action
                      0    1 - No Action
                      1    0 - Reset Special Mask
                      1    1 - Set Special Mask

                    Bit7 = 0
```

0021 8259A Interrupt Controller

```
INITIALIZATION CONTROL WORD 2
Bit0 - 7:  Not Used
Bit3 - 7:  T3 - T7 of Interrupt Vector Address
           (8086/8088 Mode)

INITIALIZATION CONTROL WORD 3 (Master Device)
Bit0 - 7:  =1   Indicated IR input has a slave
           =0   Indicated IR input does not have
                a slave

INITIALIZATION CONTROL WORD 3 (Slave Device)
Bit0 - 2 = IDO - 2
       Bit0 Bit1 Bit2 - Slave ID #
         0    0    0  -     0
         0    0    1  -     1
         0    1    0  -     2
         0    1    1  -     3
         1    0    0  -     4
         1    0    1  -     5
         1    1    0  -     6
         1    1    1  -     7
Bit3 - 7 = 0 (Not Used)

INITIALIZATION CONTROL WORD 4
Bit0:  Type of Processor
  =0   MCS-80/85 Mode
  =1   8086/8088 Mode
Bit1:  Type of End Of Interrupt
  =0   Normal EOI
  =1   Auto EOI
Bit2 - 3:  Buffering Mode
       Bit3 Bit2
         0    X    Non-buffered Mode
         1    0    Buffered Mode/Slave
         1    1    Buffered Mode/Master
Bit4:  Nesting Mode
  =0   Not Special Fully Nested Mode
  =1   Special Fully Nested Mode
Bit5 - 7:  =0 (Not Used)

OPERATION CONTROL WORD 1 (IOR*/IOW*)
Bit0 - 7:  Interrupt Mask for IRQ0 - IRQ7
  =0   Mask Reset (Enable)
  =1   Mask Set (Disable)
```

NOTE: Peripherals Requesting an interrupt service must generate a low to high edge and then remain at a logic high level service, must generate a low to high edge and then remain at a high until service is acknowledged. Failure to do so will result in a Default Service for IRQ7

0022-003F Not Used

Address	Description
0040/0044	8253-5 Timer IOW* = 0: Load Counter No. 0 IOR* = 0: Read Counter No. 0
0041/0045	8253-5 Timer IOW* = 0: Load Counter No. 1 IOR* = 0: Read Counter No. 1

Address	Description
0040/0044	8253-5 Timer IOW* = 0: Load Counter No. 0 IOR* = 0: Read Counter No. 0
0041/0045	8253-5 Timer IOW* = 0: Load Counter No. 1 IOR* = 0: Read Counter No. 1
0042/0046	8253-5 Timer IOW* = 0: Load Counter No. 2 IOR* = 0: Read Counter No. 2
0043/0047	8253-5 Timer IOW* = 0: Write Mode Word Control Word Format Bit0: BCD = 0: BCD Counter (4 Decades) = 1: Binary Counter 16 bits BIT1 - 3: Mode Selection Bit3 Bit2 Bit1 0 0 0 Mode 0 0 0 0 Mode 1 X 1 0 Mode 2 X 1 1 Mode 3 1 0 0 Mode 4 1 0 1 Mode 5 BIT4 - 5: Read/Load Bit5 Bit4 0 0 Counter Latching Operation 0 1 Read/Load LSB only 1 0 Read/Load MSB only 1 1 Read/Load LSB first, then MSB BIT6 - 7: Select Counter Bit7 Bit6 0 0 Select Counter 0 0 1 Select Counter 1 1 0 Select Counter 2 1 1 Illegal IOR* = 0: No-Operation 3-State
0048-005F	Not Used

0060 PORT A / KEYBOARD INTERFACE CONTROL PORTS (READ ONLY)

BIT	Description
0	Keyboard Bit 0-LSB
1	Keyboard Bit 1
2	Keyboard Bit 2
3	Keyboard Bit 3
4	Keyboard Bit 4
5	Keyboard Bit 5
6	Keyboard Bit 6
7	Keyboard Bit 7-MSB

0061 PORT B - READ or WRITE

BIT	Description
0	1 = 8253 Gate #2 Enable
1	1 = Speaker Data Out Enable
2	Not Used
3	Not Used
4	1 = Disable Internal Speaker (Sound Control 2)
5	0 = Sound Control 0
6	0 = Sound Control 1
7	1 = Keyboard Clear

0062 PORT C - READ/WRITE: Bits 0-3; READ ONLY: BITS 4-7

BIT	Description
0	(Output) Not Used
1	(Output) Multi-Data
2	(Output) Multi-Clock
3	(Output) CPU Clock Rate 0 = 4.77 MHz (PC Compatible Rate) 1 = 7.16 MHz (Default by Boot ROM)
4	Video Ram Size 0 = 128K Video 1 = 256K Video
5	8253 Out #2
6	Monochrome Mode 0 = Color Monitor 1 = 350 Line Monitor, Mono
7	0 = Reserved

0063-007F Not Used

Address	Description
0080	DMA Page Reg. (Not Used)

0081	WRITE ONLY
Address	**Description**
Bit 0	DMA Ch 2 Address A16
Bit 1	DMA Ch 2 Address A17
Bit 2	DMA Ch 2 Address A18
Bit 3	DMA Ch 2 Address A19
Bit 4	Not Used
Bit 5	Not Used
Bit 6	Not Used
Bit 7	Not Used

0082	WRITE ONLY
Address	**Description**
Bit 0	DMA Ch 3 Address A16
Bit 1	DMA Ch 3 Address A17
Bit 2	DMA Ch 3 Address A18
Bit 3	DMA Ch 3 Address A19
Bit 4	Not Used
Bit 5	Not Used
Bit 6	Not Used
Bit 7	Not Used

0083	WRITE ONLY
Address	**Description**
Bit 0	DMA Ch 0 - 1 Address A16
Bit 1	DMA Ch 0 - 1 Address A17
Bit 2	DMA Ch 0 - 1 Address A18
Bit 3	DMA Ch 0 - 1 Address A19
Bit 4	Not Used
Bit 5	Not Used
Bit 6	Not Used
Bit 7	Not Used

0084-008F	Not Used

00A0-00A7	NMI Mask Register, Write only
Bit	**Description**
0	External Video 0 = Normal Operation 1 = All Video Addresses and Ports are Disabled
1	MEMCONFIG 1 - A17 128K SW
2	MEMCONFIG 2 - A18 256K SW
3	MEMCONFIG 3 - A19 512K SW
4	"1" Enable 256K of Video RAM
5	Not Used
6	Not Used
7	1 = Enable NMI 0 = Disabled

BIT 4 256K Enable	BIT 3 A19	BIT 2 A18	BIT 1 A17	MEMORY START	MEMORY LENGTH	MEMORY RANGE
0	0	0	0	0 0000	128K	0 0000-1 FFFF
0	0	0	1	2 0000	128K	2 0000-3 FFFF
0	0	1	0	4 0000	128K	4 0000-5 FFFF
0	0	1	1	6 0000	128K	6 0000-7 FFFF
0	1	0	0	8 0000	128K	8 0000-9 FFFF
1	0	0	1	0 0000	256K	0 0000-3 FFFF
1	0	1	0	2 0000	256K	2 0000-5 FFFF
1	0	1	0	4 0000	256K	4 0000-7 FFFF
1	1	0	0	6 0000	256K	6 0000-9 FFFF

NOTE: To turn off on-board video, be sure Port AOH, Data Bit 0 is a "1" AND Video Array Register 3 (Selected by writing 03 into 3DAH) Data Bit 0 (Write to Port 3DEH) must be = "0" to disable 3B8H and 3BAH.

00A8 - 00AF Not Used

Address	Description
00C0-00C7	Sound SN76496

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
= 1	0	0	0	F6	F7	F8	F9	Update Tone Frequency 1
= 0	X	F0	F1	F2	F3	F4	F5	Additional Frequency Data
= 1	0	0	1	A0	A1	A2	A3	Update Tone Attenuation 1
= 1	0	1	0	F6	F7	F8	F9	Update Tone Frequency 2
= 0	X	F0	F1	F2	F3	F4	F5	Additional Frequency Data
= 1	0	1	1	A0	A1	A2	A3	Update Tone Attenuation 2
= 1	1	0	0	F6	F7	F8	F9	Update Tone Frequency 3
= 0	X	F0	F1	F2	F3	F4	F5	Additional Frequency Data
= 1	1	0	1	A0	A1	A2	A3	Update Tone Attenuation 3
= 1	1	1	0	X	FB	NF0	NFI	Update Noise Control
= 1	1	1	1	AO	A1	A2	A3	Update Noise Attenuation

00C8-00DF Not Used
00E0-01FF Reserved
WRITE (IOW*)
0200 - 0207 Joystick
Clear (Resets Integrator to Zero)
0208 - 020F Not Used

0201 READ R = Right Joystick, L = Left Joystick

Bit	Description
0	R - X Horizontal Position
1	R - Y Vertical Position
2	L - X Horizontal Position
3	L - Y Vertical Position
4	R Button #1 (Logic 0 = Button Depressed)
5	R Button #2 (Logic 0 = Button Depressed)
6	L Button #1 (Logic 0 = Button Depressed)
7	L Button #2 (Logic 0 = Button Depressed)

Addresses

0370 - 0377 Not Used

0378 Printer - Data Latch

Bit	Description
0	Data Bit 0 - LSB
1	Data Bit 1 -
2	Data Bit 2 -
3	Data Bit 3 -
4	Data Bit 4 -
5	Data Bit 5 -
6	Data Bit 6 -
7	Data Bit 7 - MSB

0379 Printer - Read Status

Bit	Description
0	Not Used
1	Not Used
2	Not Used
3	0 = Error
4	1 = Printer Select
5	0 = End of Form
6	0 = Acknowledge
7	0 = Busy

037A (037E) Printer - Control Latch

Bit	Description
0	0 = Strobe
1	0 = Auto FD XT
2	0 = Initialize
3	0 = Select Printer
4	1 = Enable Interrupt
5	0 = Enable Output Data
6	Not Used
7	Not Used

037B	Not Used
037C	Printer - Data Latch
037D	Printer - Read Status
037F - 03D3	Not Used
03D4	6845 Address Register
03D5	6845 Data Register
03D6	Not Used
03D7	Not Used
03D8	Mode Select Register
Bit 0	High Resolution Clock =0: Selects 40 by 25 Alphanumeric Mode =1: Selects 80 by 25 Alphanumeric Mode
Bit 1	Graphics Select =0: Selects Alphanumeric Mode =1: Selects 320 by 200 Graphics Mode
Bit 2	Black and White =0: Selects Color Mode =1: Selects Black and White Mode
Bit 3	Video Enable =0: Disables Video Signal =1: Enables Video Signal
Bit 4	640 Dot Graphics =0: Disables 640 by 200 B&W Graphics Mode =1: Enables 640 by 200 B&W Graphics Mode
Bit 5	Blink Enable =0: Disables Blinking =1: Enables Blinking
03D9	Color Select Register
Bit 0	Background Blue
Bit 1	Background Green
Bit 2	Background Red
Bit 3	Background Intensity
Bit 4	Foreground Intensity
Bit 5	Color Select
03DA, 03DE	Write Video Array Address & Read Status (3DA) Write Video Array Data (3DE)

READ (3DA)		WRITE (3DE)
00 Bit 0	Display Inactive	Not Used
00 Bit 1	Light Pen Set	Not Used
00 Bit 2	Light Switch Status	Not Used
00 Bit 3	Vertical Retrace	Not Used
00 Bit 4	Not Used	Not Used
01 Bit 0		Palette Mask 0
01 Bit 1		Palette Mask 1
01 Bit 2		Palette Mask 2
01 Bit 3		Palette Mask 3
02 Bit 0		Border Blue
02 Bit 1		Border Green
02 Bit 2		Border Red
02 Bit 3		Border Intensity
02 Bit 5		Reserved = 0
03 Bit 0		Mono Enable = "1"
03 Bit 1		Reserved = 0
03 Bit 2		Border Enable
03 Bit 3		4-Color High Resolution
03 Bit 4		16 Color Mode
03 Bit 5		Extra Video Mode
10-1F Bit 0		Palette Blue
10-1F Bit 1		Palette Green
10-1F Bit 2		Palette Red
10-1F Bit 3		Palette Intensity
Bits 4 - 7		Not Used

03DB Clear Light Pen Latch (Not Used on Tandy 1000 EX)
03DC Preset Light Pen Latch (Not Used on Tandy 1000 EX)

03DD Extended Ram Page Register - CPU Relative

Bit	Description
0	Extended Addressing Modes
1	Not Used
2	Not Used
3	CRT Video Page Address "17"
4	CRT Video Page Address "18"
5	CPU Page Address "17"
6	CPU Page Address "18"
7	Select 64K or 256K Ram

```
03DF              CRT Processor Page Register - Video Mem Relative
 Bit 0            A14                CRT Page 0
 Bit 1            A15                CRT Page 1
 Bit 2            A16                CRT Page 2
 Bit 3            A14                Processor Page 0
 Bit 4            A15                Processor Page 1
 Bit 5            A16                Processor Page 2
 Bit 6                               Video Address Mode 0
 Bit 7                               Video Address Mode 1

03F1              Drive Select Switch
                  "1" DS0 = DS0
                  "0" DS0 = DS1
03F2, 3F0, 3F3    DOR Register (Write Only)
                  Bit0 - 1:  Drive Select
                    Bit1 Bit0
                      0    0          Drive Select A*
                      0    1          Drive Select B*
                  Bit2:  0 = FDC Reset
                  Bit3:  1 = Enable DMA Req/Interrupt
                  Bit4:  1 = Drive A Motor On
                  Bit5:  1 = Drive B Motor On
                  Bit6:  1 = FDC Terminal Count
                  Bit7:  Not Used

03F4, 3F6         FDC - Status (Read Only) - See FDC Specification
03F5, 3F7         FDC - Data (R/W) - See FDC Specification
03F8 - 03FF       Not Used

For Ports 3F0 - 3F7, the following general conditions apply:
                  A1 = Don't Care
                  For DOR, A2 = 0
                  For FDC, A2 = 1
```

DATA	IBM PC 0062 -- PORT C -- READ ONLY	IBM PCjr 0062 -- PORT C -- READ ONLY	TANDY 1000 EX 0062 -- PORT C --
BIT 0	CONFIG SW16 OR (R/W)	1 = KEYBOARD LATCHED	(OUT) NOT USED
	CONFIG SW12 (R/W)		
	SEE PORT 0061, BIT 2 (R/W)		
BIT 1	CONFIG SW15 (R/W)	0 = INTERNAL MODEM INSTALLED	(OUT) MULTI-DATA
BIT 2	CONFIG SW14 (R/W)	0 = DISKETTE DRIVE INSTALLED	(OUT) MULTI-CLOCK
BIT 3	CONFIG SW13 (R/W)	0 = 64K RAM EXPANSION	FAST (0=STD OPERATION) read/write "0"=4.77MHz "1"=7.16MHz
		INSTALLED	read/write "0"=4.77MHz "1"=7.16MHz
BIT 4	CASSETTE DATA IN (R)	SAME VIDEO	RAM SIZE READ ONLY 0=128K VIDEO 1=256K VIDEO
BIT 5	8253 OUT #2 (R)	SAME	(IN) SAME
BIT 6	1=I/O CHECK (PARITY ERROR) (R)	KEYBOARD DATA	MONOCHROME MODE 0=COLOR MONITOR 1=350 LINE MONITOR MONO
BIT 7	1=RAM PARITY ERROR (R)	KEYBOARD CABLE INSTALLED	RESERVED = 0
	HARDWARE LOGIC ATTACHED IS FOR INPUT ONLY.		IN TANDY 1000 THE HARDWARE LOGIC IS CONFIGURED SO THAT PORT C IS SPLIT WITH INPUT: PC4 -- PC7 OUTPUT: PC0 -- PC3

DATA	IBM PC 0061 -- PORT B -- READ OR WRITE	IBM PCjr 0061 -- PORT B -- READ OR WRITE	TANDY 1000 0061 -- PORT B -- READ OR WRITE
BIT 0	1=8253 GATE #2 ENABLED	SAME	SAME
BIT 1	SPEAKER DATA OUT	SAME	SAME
BIT 2	1=ENABLE READING	1=ALPHA (GRAPHICS)	NO FUNCTION
|	CONFIG SW13 THRU 16		
|	(I/O CHAN ROM SIZE) OR		
|	0=ENABLE READING		
V	CONFIG SW12 (@PC0 -- PC3)		
BIT 3	1=CASSETTE MOTOR OFF	SAME	NO FUNCTION
BIT 4	0=ENABLE RAM PARITY	1=DISABLE CASSETTE MTR RELAY, INTERNAL BEEPER	1=DISABLE INTERNAL SPEAKER (SOUNDCONT2)
BIT 5	0=ENABLE I/O CH PARITY	SPKR SW 0	SOUND CONTROL 0
BIT 6	0=HOLD KEYBOARD CLK LOW	SPKR SW 1	SOUND CONTROL 1
BIT 7	0=ENABLE KEYBOARD	1=KEYBOARD CLEAR	1=KEYBOARD CLEAR
|	1=CLEAR KEYBOARD AND		
V	ENABLE CONFIG SW 1-8		

VIDEO / SYSTEM MEMORY ADDRESS MAP

0A0 BIT 4	MC3 0A0 BIT 3 A19	MC2 0A0 BIT 2 A18	MC1 0A0 BIT 1 A17	VIDEO/SYSTEM MEMORY START ADDRESS	VIDEO/SYSTEM MEMORY LENGTH	VIDEO/SYSTEM MEMORY ADDRESS RANGE
0*	0	0	0	00000 (0)	128K	00000-1FFFF
0	0	0	1	20000 (128K)	128K	20000-3FFFF
0	0	1	0	40000 (256K)	128K	40000-5FFFF
0	0	1	1	60000 (324K)	128K	60000-7FFFF
0	1	0	0	80000 (512K)	128K	80000-9FFFF
1	0	0	1	00000 (0)	256K	00000-3FFFF
1	0	1	0	20000 (128K)	256K	20000-5FFFF
1	0	1	1	40000 (156K)	256K	40000-7FFFF
1	1	0	0	60000 (384K)	256K	60000-9FFFF

* ENDBIP 256K OF VIDEO ROM IF "1"

Tl000 EX Main Logic Subassembly		8859000
Symbol	Description	Number
Tandy 1000 EX Main Logic PCB Rev. A (11.4 X 8.4)		8709689A
C1,4-7,9-16,15A, 18-24,26-39,78, 104-108,111,112, 117,128,166,171	Capacitor 0.1 MFD 50V Axial	8374104
C41-48	Capacitor .33 MFD 50V Mono. Ax.	8374334
C100	Capacitor 100 PF 50V C. Disk	8301104
C101,130,167	Capacitor 10 MFD 16V Elec Ax.	8316101
C102,103,110,114, 133,134,169	Capacitor 22 MFD 16V Elec Ax.	8316221
C109	Capacitor 2.2 MFD 16V Elec Ax.	8315221
C113,165,173-177	Capacitor 470 PFD 50V C. Disk	8301474
C115	Capacitor 100 MFD 16V Elec Ax.	8317101
C116,126,129,131, 136,138,170	Capacitor 1000 PFD 50V C. Disk	8302104
C118-125	Capacitor 68 PFD 50V C. Disk	8300684
C127	Capacitor .022 MFD 63V 10% Poly	8393225
C132,135,168,172	Capacitor .47 MFD 50V Mono. Rad.	8384475
C137	Capacitor 180 PFD 50V C. Disk	8301184
C139-141,144-146, 153	Capacitor 20 PF 50V C. Disk	8300204
C142,143,147-152	Capacitor 2200 PFD C. Disk	8302224
C154-156,159-164	Capacitor 220 PFD 50V C. Disk	8301223
CR1,2	Diode 1N4148	8150148
CR3	Diode 1N5235 6.8V	8150235
E1,2	Staking Pins	8529014
FB1,2	Ferrite Bead	8419013
J1	Connector, 2-Pin Header, Spkr.	8519193
J2	Connector, 6-Pin (Kybd Led)	8519293
J3,4	Connector, 12-Pin Flat Flex ZIF	8519309
J5	Connector, 2-Pin Header Rt. Angle Fan	8519308
J6	Connector, 6-Pin Power Rt. Ang. (Rev. A Only)	8519186
J6	Connector, 6-Pin Power (Rev B)	8519281
J7	Connector, 13-Pin Flat Flex ZIF	8519310
J8	Connector, Sub Mini Jack	8519282
J9,10	Connector, 6-Pos. Rt. Angle	8519289
J11	Connector, Dual 17-Pin Straight	8519120
J12	Connector, Dual 31-Pin Straight I/O Pin Header .687" Ht	8519290
J15	Connector, Single Plug	8519287

Symbol	Description	Number
J16	Connector, 9-Pin Rt. Angle, Female "D" Sub	8519245
J16	Nut, #4-40 KEPS	8579003
J16	Screw, #4-40 X 3/8"	8569002
Q1	Transistor 2N3906	8100906
Q2	Transistor VMOS	8190104
Q3	Transistor 2N3904	8110904
R1	Resistor, Variable 1K	8279209
R2	Resistor 3.9K Ohm 1/4 Watt 5%	8207239
R3,35	Resistor 10 Ohm 1/4 Watt 5%	8207010
R4-6	Resistor 180 Ohm 1/4 Watt 5%	8207118
R7,15,31,32,46, 48	Resistor 4.7K Ohm 1/4 Watt 5%	8207247
R8,18,41,49,55	Resistor 2.2K Ohm 1/4 Watt 5%	8207222
R9,59	Resistor 680 Ohm 1/4 Watt 5%	8207168
R10	Resistor 2.7K Ohm 1/4 Watt 5%	8207227
R13-14,17,19-21, 23,25,28,29,42, 44,50	Resistor 10K Ohm 1/4 Watt 5%	8207310
R16	Resistor 330 Ohm 1/4 Watt 5%	8207133
R22	Resistor 82.5K Ohm 1/4 Watt 1%	8200382
R24,26,33,43	Resistor 1 Meg Ohm 1/4 Watt 5%	8207510
R27,45	Resistor 560 Ohm 1/4 Watt 5%	8207156
R29A,37-40	Resistor 39 Ohm 1/4 Watt 5%	
R30,51	Resistor 1K Ohm 1/4 Watt 5%	8207210
R34	Resistor 47K Ohm 1/4 Watt 5%	8207347
R36	Resistor 680K Ohm 1/4 Watt 5%	8207468
R47,51A,51B,61-64	Resistor 33 Ohm 1/4 Watt 5%	8207033
R52	Resistor 470 Ohm 1/4 Watt 5%	8207147
R53	Resistor 620 Ohm 1/4 Watt 5%	8207162
R54	Resistor 270 Ohm 1/4 Watt 5%	8207127
R56	Resistor 1.2K Ohm 1/4 Watt 5%	8207212
R57	Resistor 1.1K Ohm 1/4 Watt 5%	8207211
R58	Resistor 750 Ohm 1/4 Watt 5%	8207175
R60	Resistor 3.3K Ohm 1/4 Watt 5%	8207233
R65	Resistor 75 Ohm 1/4 Watt 5%	8207075
RP1	Resistor Pak 33K Ohm 10-Pin SIP	8290064
RP2	Resistor Pak 10K Ohm 6-Pin SIP	8290032
RP3	Resistor Pak 1K Ohm 6-Pin SIP	8290210
RP4	Resistor Pak 10K Ohm 10-Pin SIP	8290010
RP5	Resistor Pak 33 Ohm 16-Pin DIP	8290044
RP6	Resistor Pak 4.7K Ohm 8-Pin SIP	8292246
RP7	Resistor Pak 150 Ohm 6-Pin SIP	8290012
RP8-10	Resistor Pak 33 Ohm 8-Pin SIP	8295033

Symbol	Description	Number
U1	IC 14529	8030529
U2,36	IC 7416	8000016
U3,11,13	Socket 20-Pin DIP	8509009
U4	LM386 Audio Amp	8050386
U5,33,35	IC 74HCT04	8026004
U6,10,14,16,27,32	Socket 40-Pin DIP	8509002
U7	Socket 24-Pin DIP	8509001
U9,17	Socket 28-Pin DIP	8509007
U11,13	IC 74HCT245	8026245
U12,18,23	IC 74HCT244	8026244
U15	Socket 16-Pin DIP	8509003
U19,20	IC HCT373	8026373
U22,39	IC 74HCT32	8026032
U24	IC 74HCT138	8026138
U26	IC 74HCT195	8026195
U28	Socket 84-Pin PLCC	8509031
U29	Socket 8-Pin DIP	8509011
U30	IC 74HCT08	8026008
U31	IC 7417	8000017
U34	IC 74HCT02	8026002
U37	IC 74HCT14	8026014
U38	IC 74LS244	8020244
U41-48	Socket 18-Pin DIP	8509006
VR1	Regulator 78L05	8052805
Y1	Oscillator 16 MHz	8409034
Y2	Oscillator 28.63636 MHz 50 PPM	8409039

**Note: U8, U40, C8, C40, R11 & R12 Are Blank

Main Logic Tl000 EX Board Main Assembly

Symbol	Description	Number
	Tandy 1000 EX Sub Assy.	8859000
	Jumper Plugs	8519098
U3	IC PLS153	8040048
U6	IC 8048	8040048
U7	IC 8253-5	8040253
U9	IC 8259A	8040259
U10	IC Keyboard I/F	8075069
U14	IC 8088 (8 MHz) CPU	8041088
U15	IC 76496	8040496
U16	IC CPU Support (Lt. Blue)	8075306
U17	IC 128K ROM	8040328
U27	IC FDC UPD765	8040272
U28	IC Big Blue	8040684
U29	IC FDC 9216	8040216
U32	IC Custom Printer Array	8041087
U41-48	IC 64K X 4 Dram 150NS	8040464

Main Logic Schematic Cuts, Jumpers and Additional Parts

.0033 µf capacitor added to U16 (Timing Controller Chip) between Pin 15 (PWR) and Pin 26 (GND).

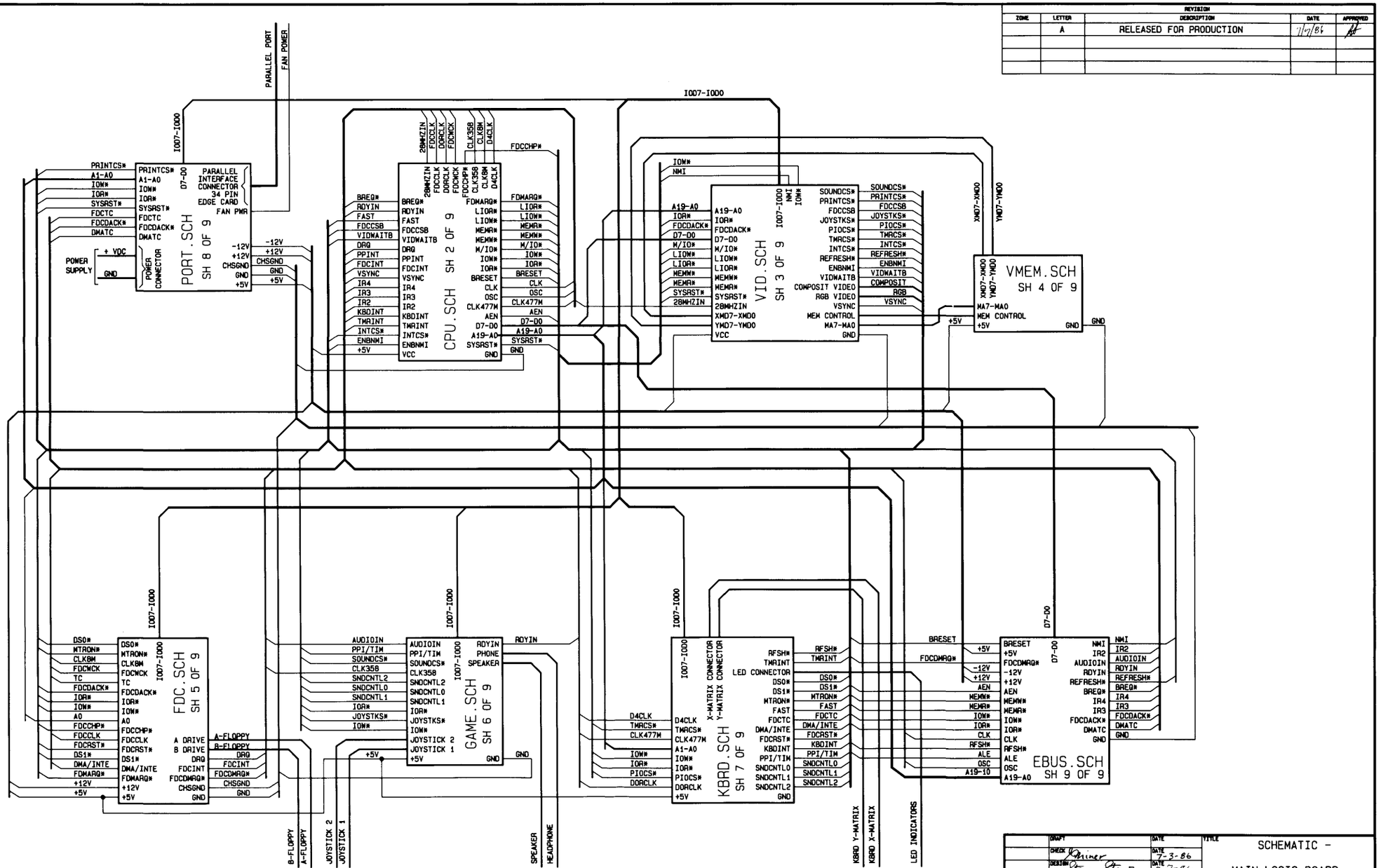
33 pf capacitor added between R47 (side connected to Video Controller Chip) and ground.

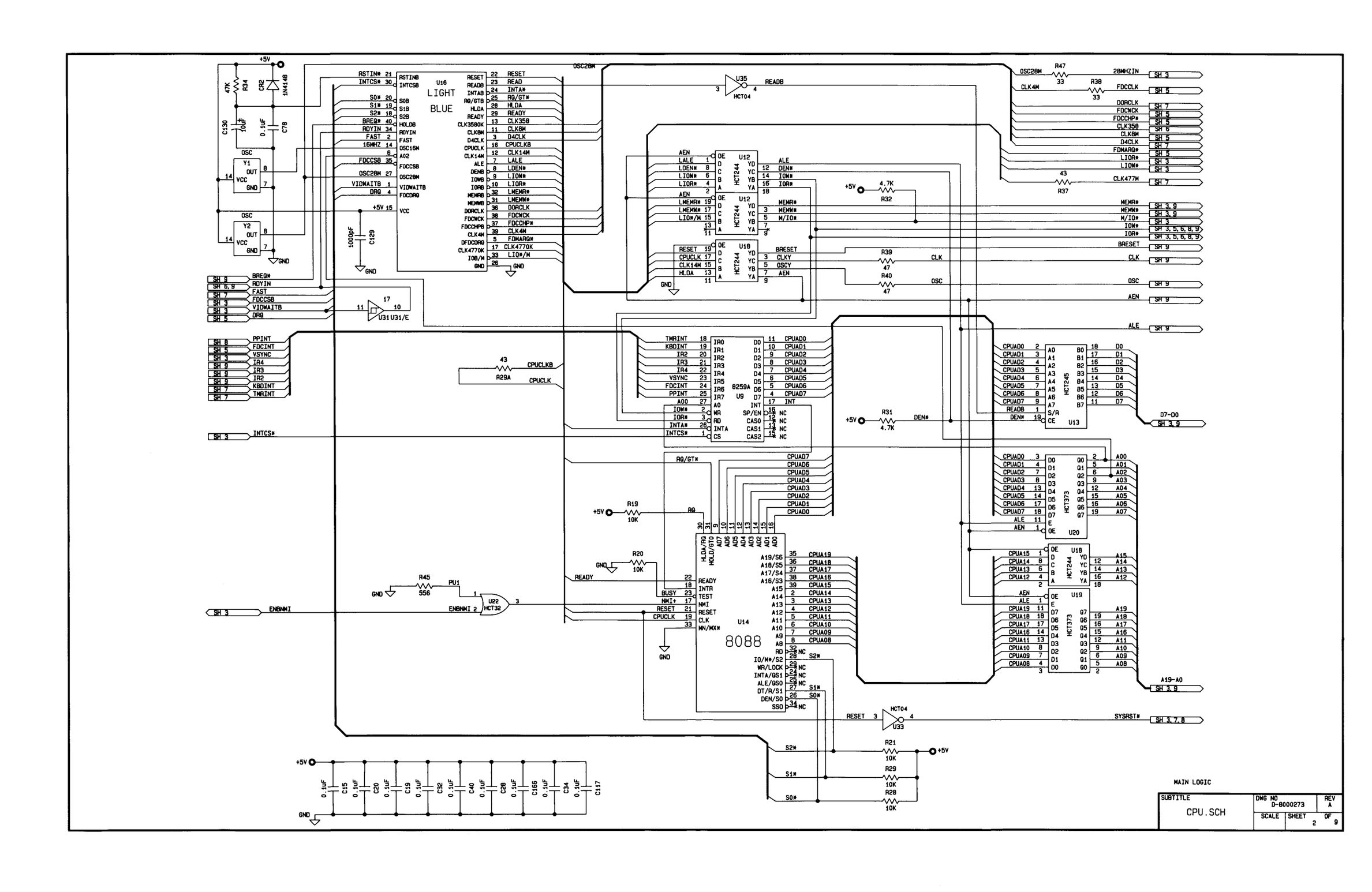
1000 pf capacitor (P/N 8302104) added in parallel with C28.

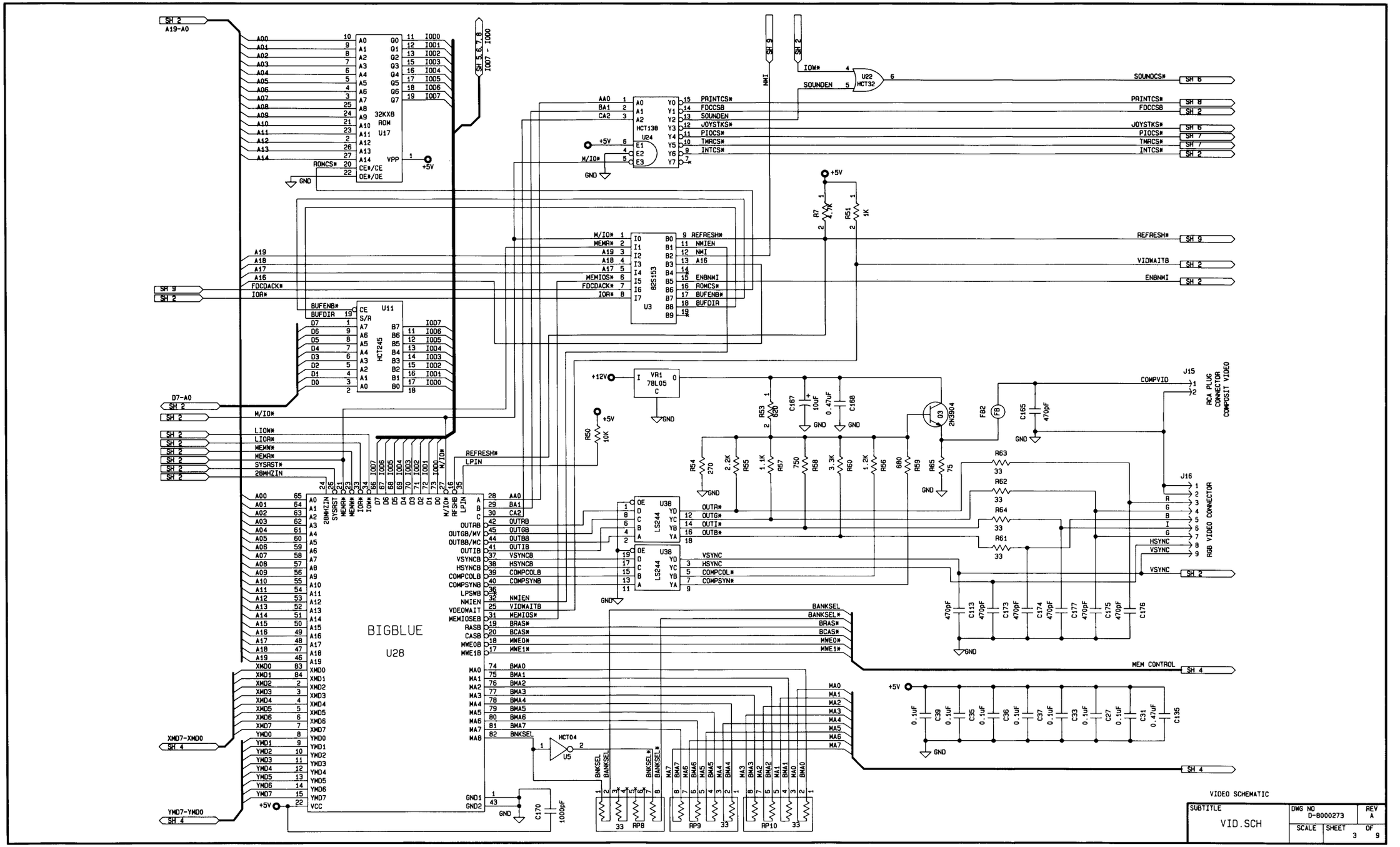
47 pf capacitor added between R39 (in parallel with side connected to Bus) and ground.

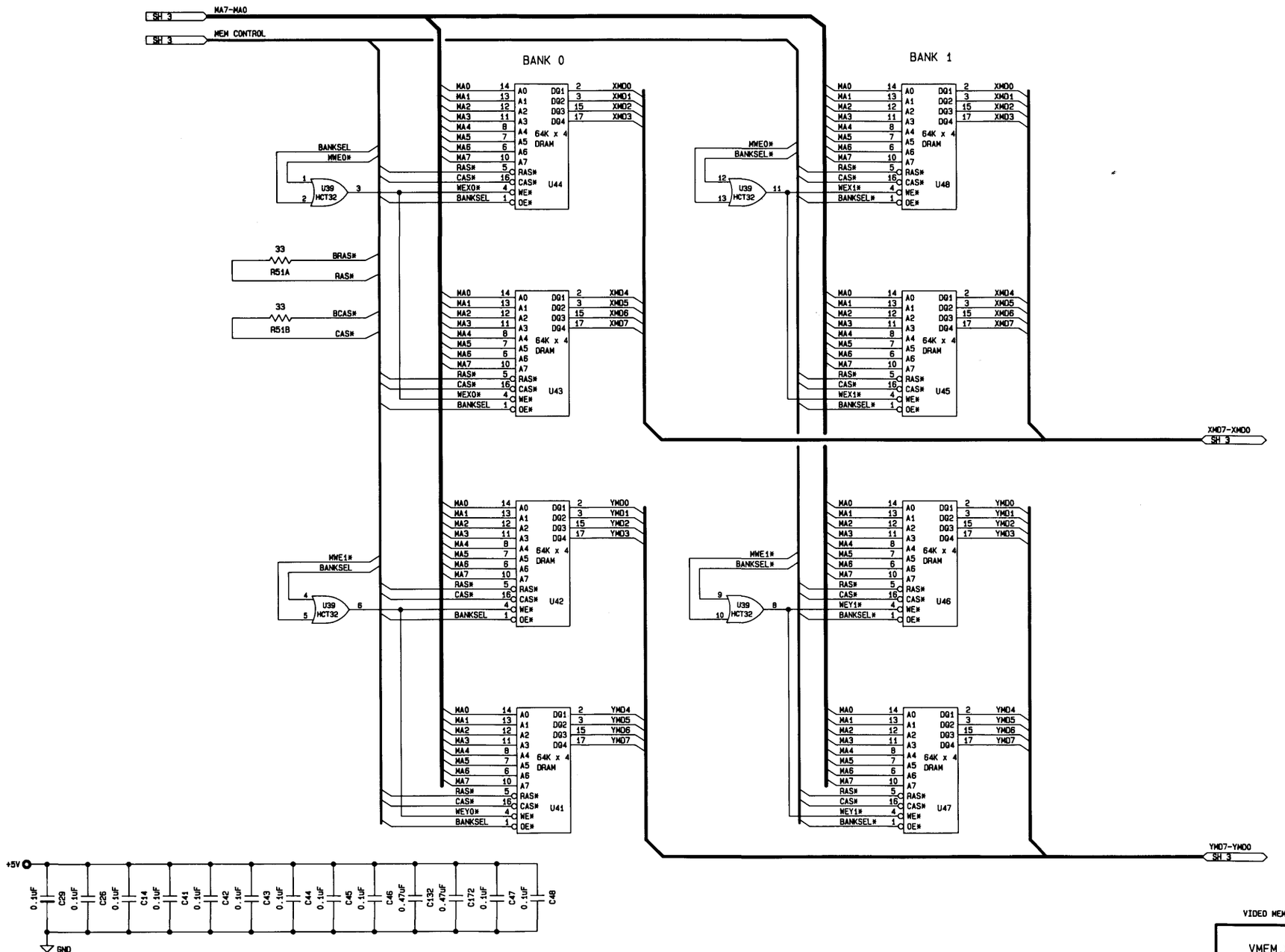
47 pf capacitor added between R40 (side connected to Bus) and ground.

Cut Pin 12 of IC MC14529 from the PCB and then Short (solder) Pin 12 to Pin 13.


REVISION
ZONE | LETTER | DESCRIPTION | DATE | APPROVED
A | RELEASED FOR PRODUCTION | 11/7/86
PARALLEL PORT
FAN POWER
IO07-IO00
PORT.SCH SH 8 OF 9
PARALLEL INTERFACE CONNECTOR 34 PIN EDGE CARD
FAN PWR
POWER SUPPLY
CPU.SCH SH 2 OF 9
VID.SCH SH 3 OF 9
VMEM.SCH SH 4 OF 9
FDC.SCH SH 5 OF 9
GAME.SCH SH 6 OF 9
KBRD.SCH SH 7 OF 9
X-MATRIX CONNECTOR
Y-MATRIX CONNECTOR
LED CONNECTOR
EBUS.SCH SH 9 OF 9
A-FLOPPY
B-FLOPPY
JOYSTICK 2
JOYSTICK 1
SPEAKER
HEADPHONE
KBRD Y-MATRIX
KBRD X-MATRIX
LED INDICATORS
DRAFT
CHECK Steiner 7-3-86
DESIGN Steve Stone 7-7-86
APPD 7/7/86
APPD 7/7/86
SCHEMATIC -
MAIN LOGIC BOARD
TANDY
620
DWG NO D- 8000273
REV A
SCALE
SHEET 1 OF 9

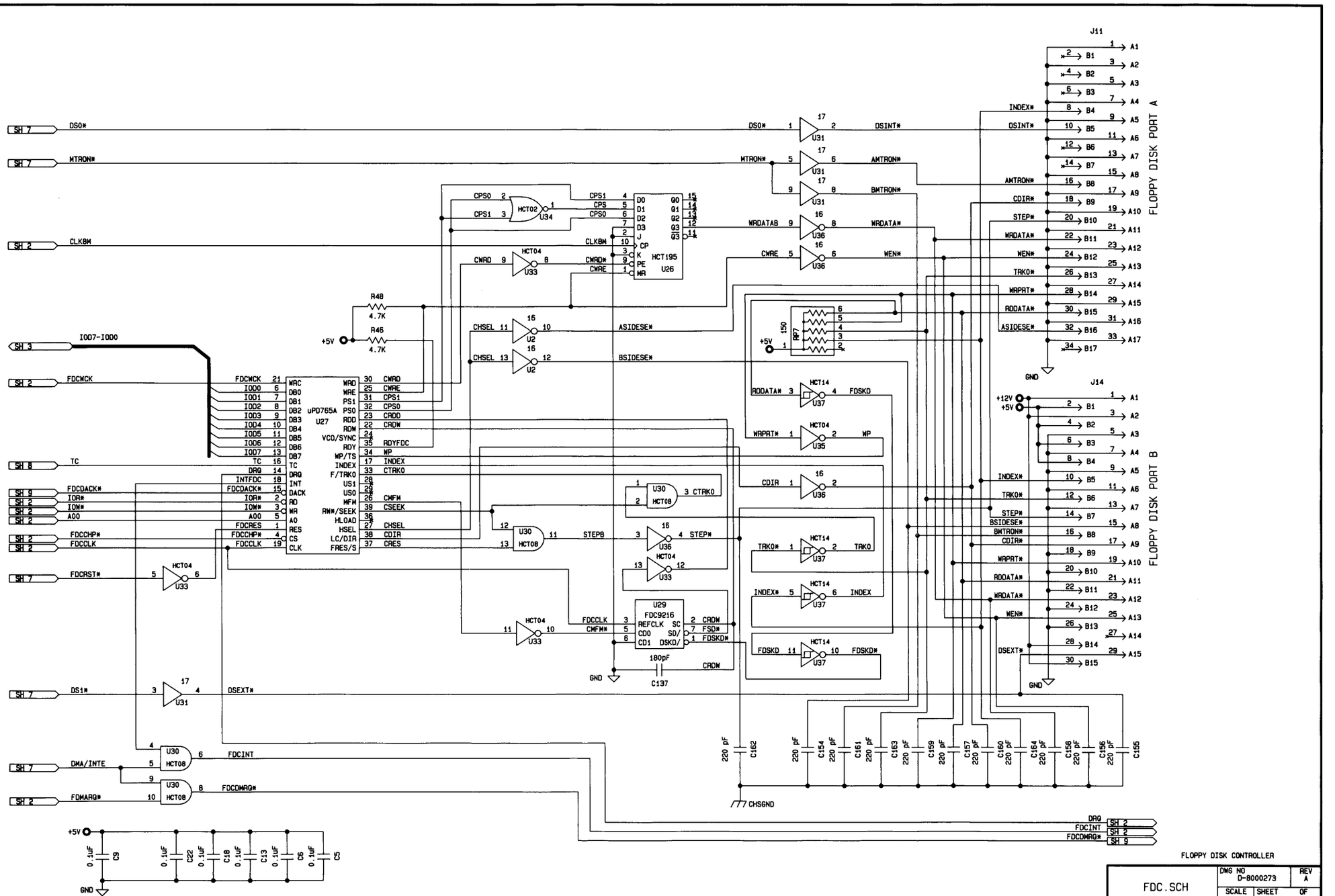

LIGHT BLUE
U16
8088
U14
8259A
U9
HCT244
HCT245
HCT373
HCT04
HCT32
MAIN LOGIC
SUBTITLE
CPU.SCH
DWG NO
D-8000273
REV
A
SCALE
SHEET
2
OF
9

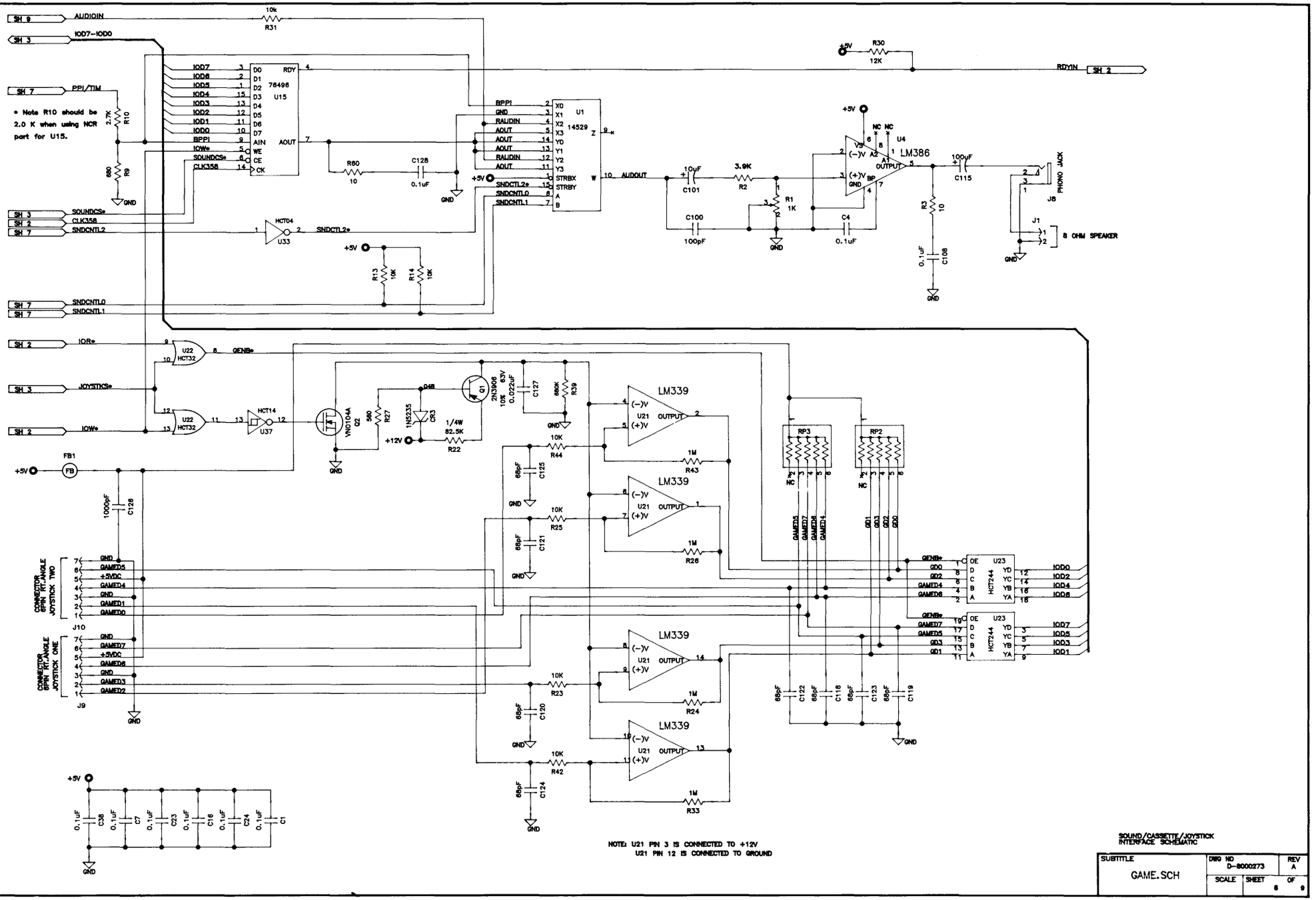

BIGBLUE
U28
VIDEO SCHEMATIC
SUBTITLE
VID.SCH
DWG NO
D-8000273
REV
A
SCALE
SHEET
3
OF
9



VIDEO MEMORY

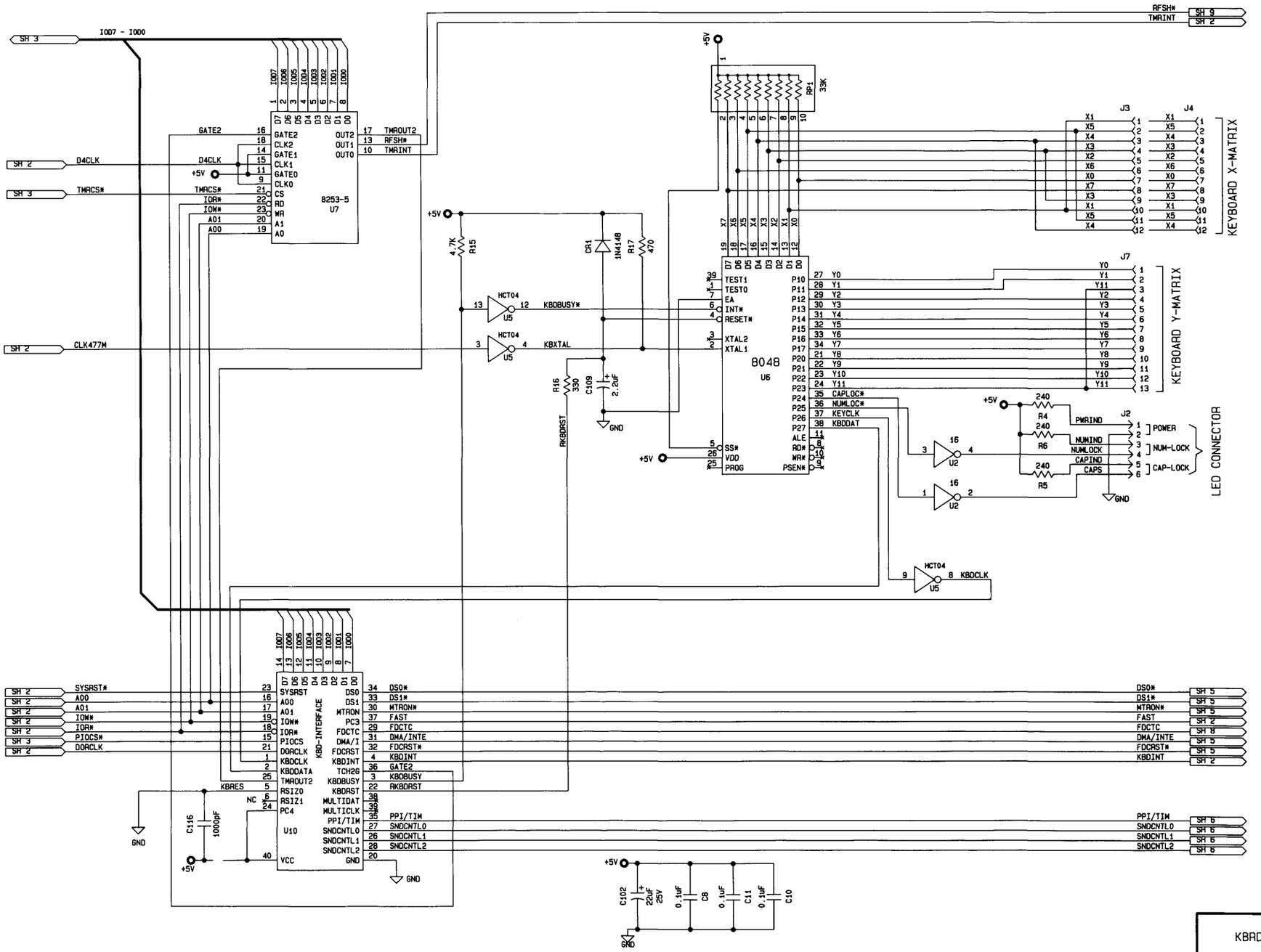
VMEM.SCH	DWG NO D-8000273	REV A
	SCALE	SHEET 4 OF 9

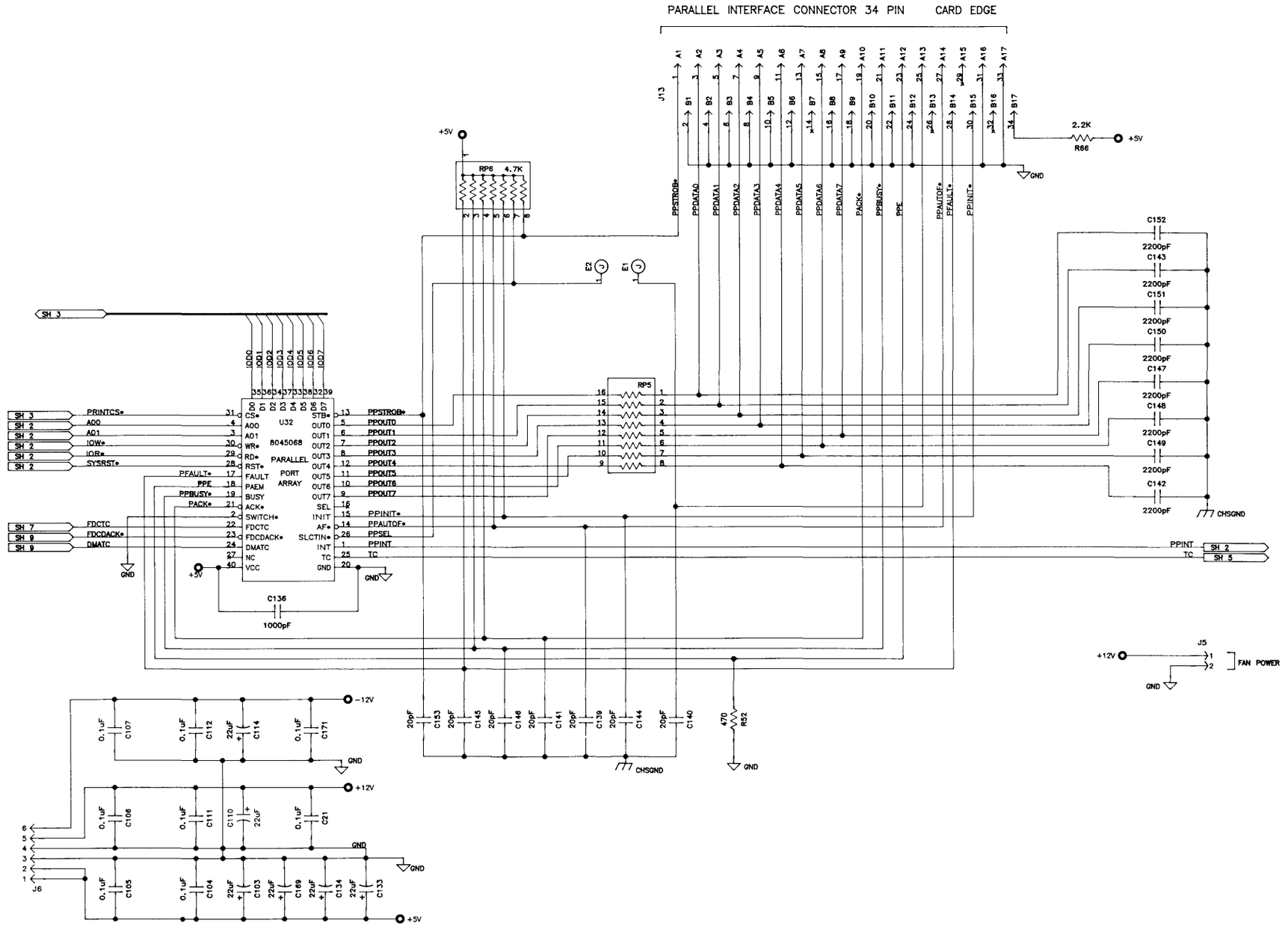

FLOPPY DISK CONTROLLER
FDC.SCH
DWG NO D-8000273
REV A
SCALE
SHEET 5 OF 9
FLOPPY DISK PORT A
FLOPPY DISK PORT B
J11
J14
uPD765A
U27
HCT195
U26
FDC9216
U29
HCT08
HCT04
HCT14
HCT02
HCT157
U2
U31
U33
U34
U35
U36
U37
RP7
DS0*
MTRON*
CLK8M
IOD7-IOD0
FDCWCK
TC
FDCDACK*
IOR*
IOW*
A00
FDCRES
FDCCHP*
FDCCLK
FDCRST*
DS1*
DMA/INTE
FDMARQ*
DSINT*
AMTRON*
BMTRON*
WRDATAB
WRDATA*
CWRE
WEN*
CHSEL
ASIDESE*
BSIDESE*
CWRD
CRDW
CMFM*
CSEEK
CDIR
CRES
STEPB
STEP*
TRK0*
TRK0
INDEX*
INDEX
WRPRT*
WP
RDDATA*
FDSKD
FDSKD*
FSD*
DSEXT*
FDINT
FDCDMRQ*
DRQ
R48
R46
4.7K
150
180pF
C137
CHSGND
GND
+5V
+12V
0.1uF
220 pF



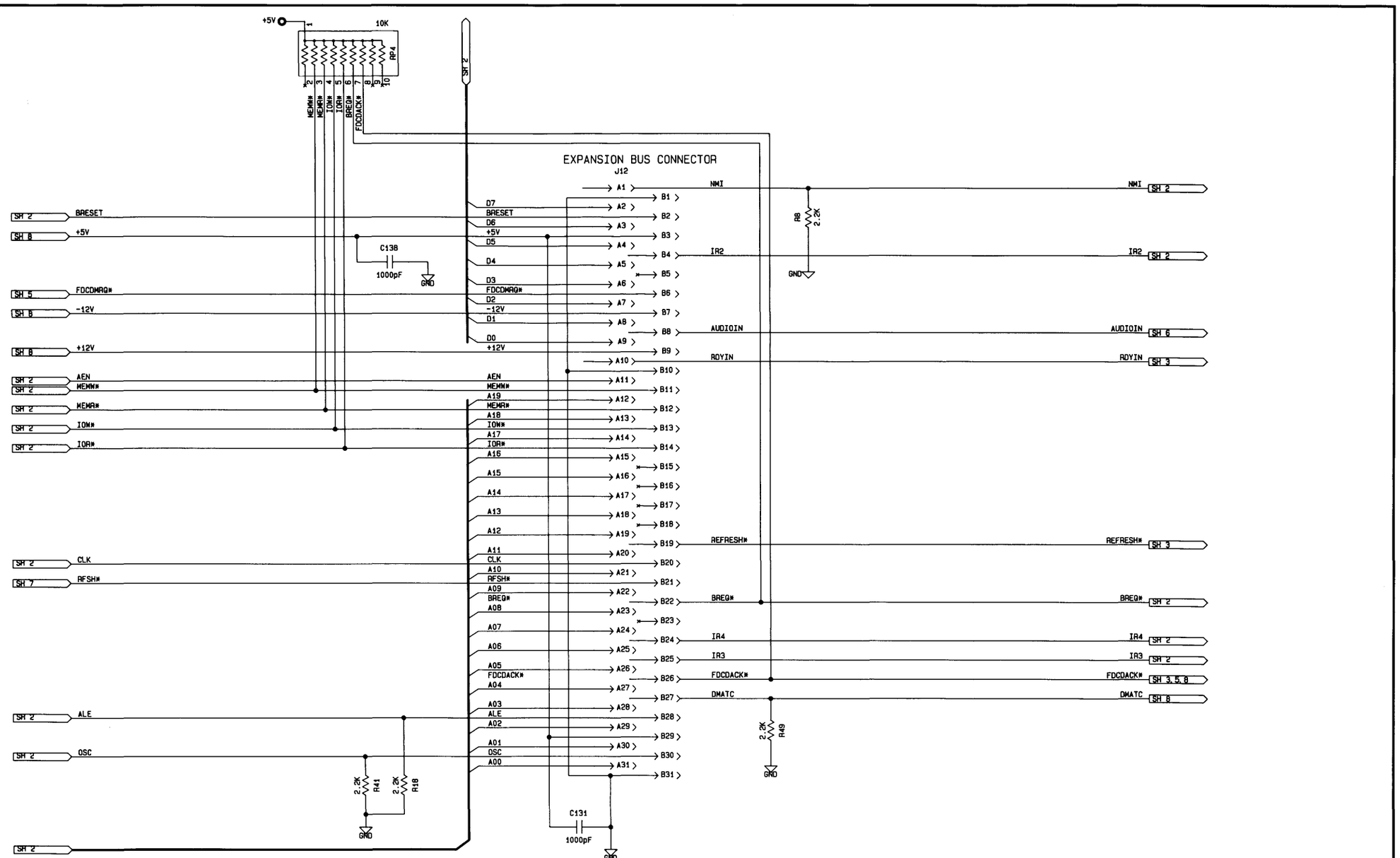
SOUND/CASSETTE/JOYSTICK INTERFACE SCHEMATIC

SUBTITLE	DWG NO	REV
GAME.SCH	D-8000273	A
	SCALE	SHEET 6 OF 9


KEYBOARD INTERFACE
KBRD.SCH
DWG NO D-8000273
REV A
SCALE
SHEET 7 OF 9
8253-5 U7
8048 U6
KBD-INTERFACE U10
KEYBOARD X-MATRIX
KEYBOARD Y-MATRIX
LED CONNECTOR
POWER
NUM-LOCK
CAP-LOCK
IOD7 - IOD0
D4CLK
TMRCS*
CLK477M
SYSRST*
DORCLK
PIOCS*
KBRES
AFSH*
TMRINT
KBDBUSY*
KBXTAL
KBDCLK
KBDDAT
KBDINT
PPI/TIM
SNDCNTL0
SNDCNTL1
SNDCNTL2
DS0*
DS1*
MTRON*
FAST
FDCTC
DMA/INTE
FDCRST*
PWRIND
NUMIND
CAPIND
NUMLOCK
CAPS
AKBDRST
+5V
GND
HCT04
1N4148
33K
4.7K
470
330
240
2.2uF
22uF 25V
0.1uF
1000pF



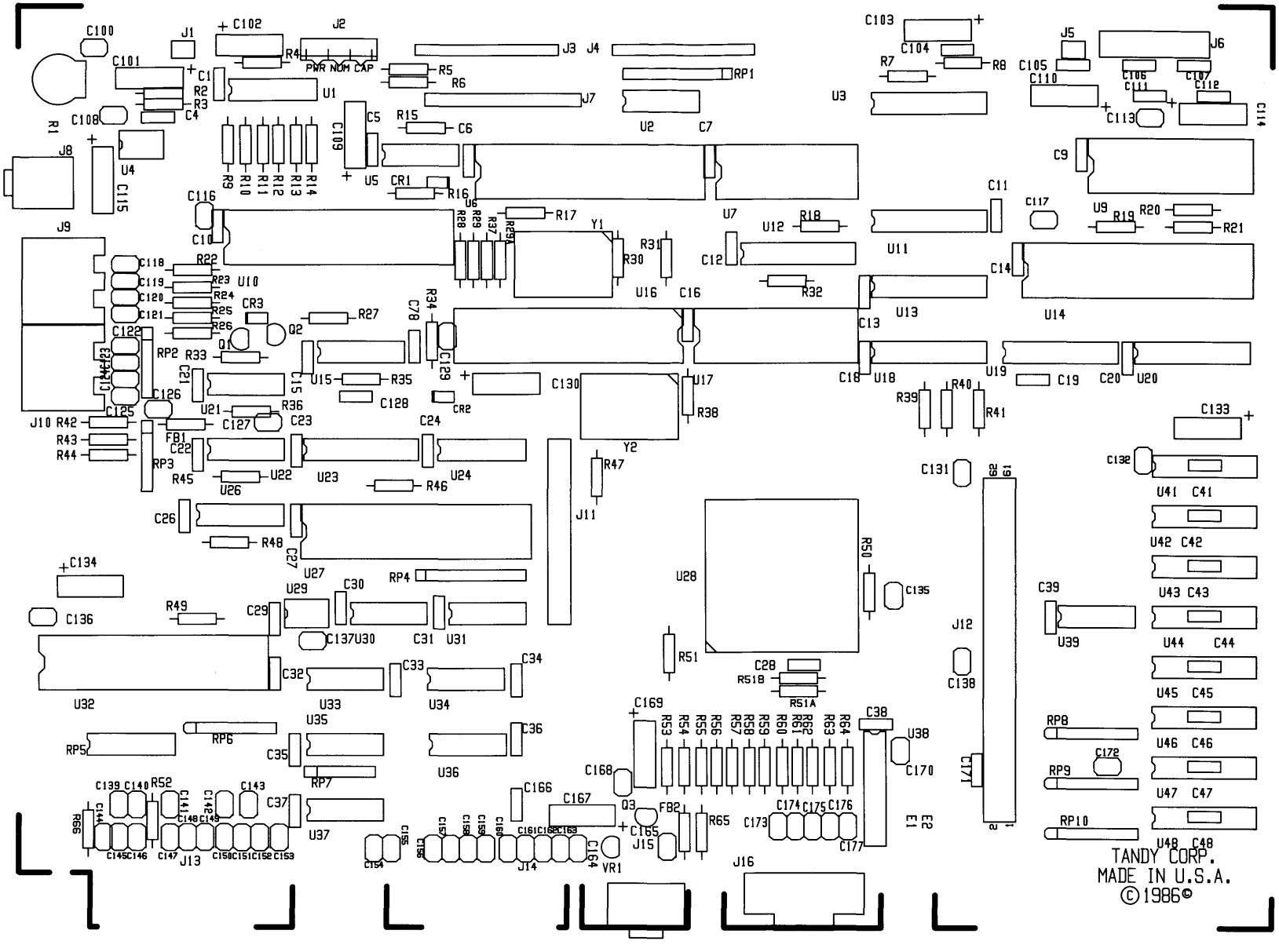
SUBTITLE PORT.SCH	DWG NO D-8000273		REV A
	SCALE	SHEET 8	OF 9



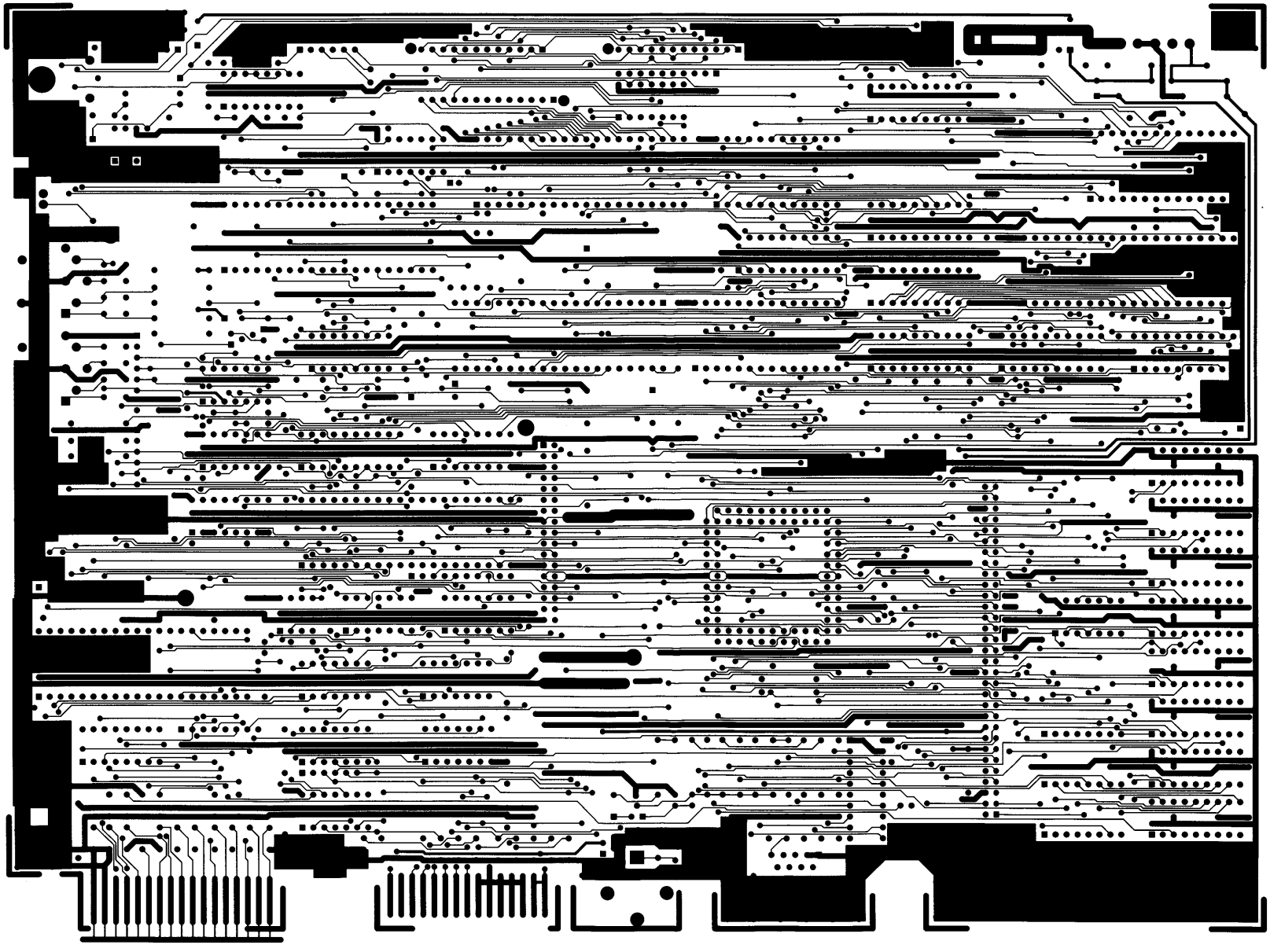
EXPANSION BUS

SUBTITLE	DWG NO	REV
EBUS.SCH	D-8000273	A
	SCALE / SHEET 9 OF 9	

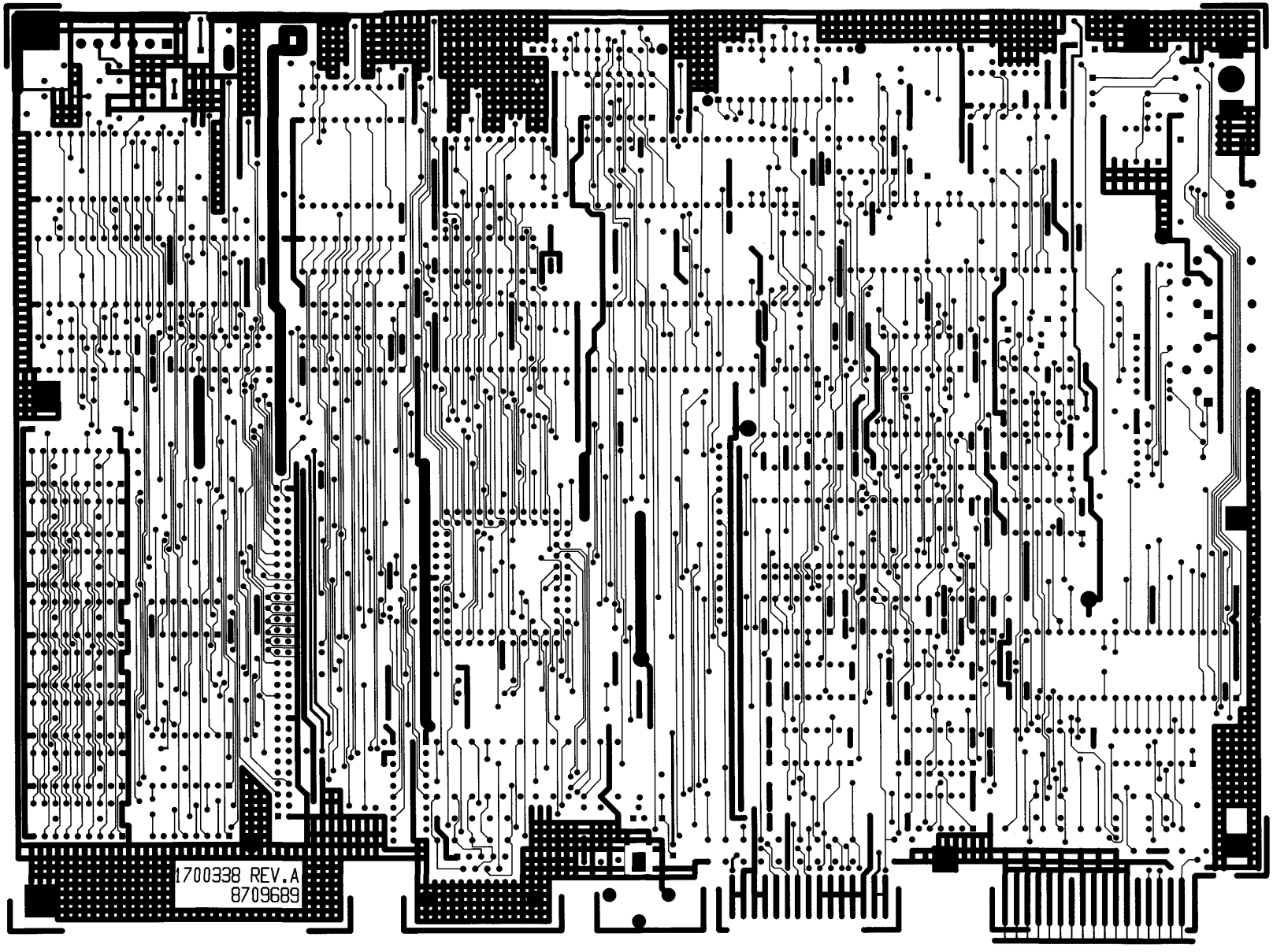
TANDY SYSTEMS DESIGN FILMWORK	FAB. SPEC.: TSD-C262-0
PROJECT NO.: 620 DATE: 5/30/86	C/S SILKSCREEN
TITLE: MAIN LOGIC BD.	
DWG. NO.: 1700338 REV. A	
PART NO.: 870-9689	
DESIGN GRID: x=.020 y=.021	
DESIGNER: VH GM DD	
INSP	



TANDY SYSTEMS DESIGN FILMWORK	FAB. SPEC.: TSD-C262-0
PROJECT NO.: 620 DATE: 5/30/86	LAYER 1 COMPONENT SIDE
TITLE: MAIN LOGIC BD.	
DWG. NO.: 1700338 REV.A	
PART NO.: 870-9689	
DESIGN GRID: x=.020 y=.021	
DESIGNER: VH | GM | DD	
INSP	



TANDY SYSTEMS DESIGN FILMWORK	FAB. SPEC.: TSD-C262-0
PROJECT NO.: 620 DATE: 5/30/86	LAYER 2 SOLDER SIDE
TITLE: MAIN LOGIC BD.	
DWG. NO.: 1700338 REV. A	
PART NO.: 870-9689	
DESIGN GRID: x=.020 y=.021	
DESIGNER: VH GM BD	
INSP	



1000 EX POWER SUPPLIES
(SINGLE AND DUAL INPUT)

1000 EX 28 Watt Single Input Power Supply

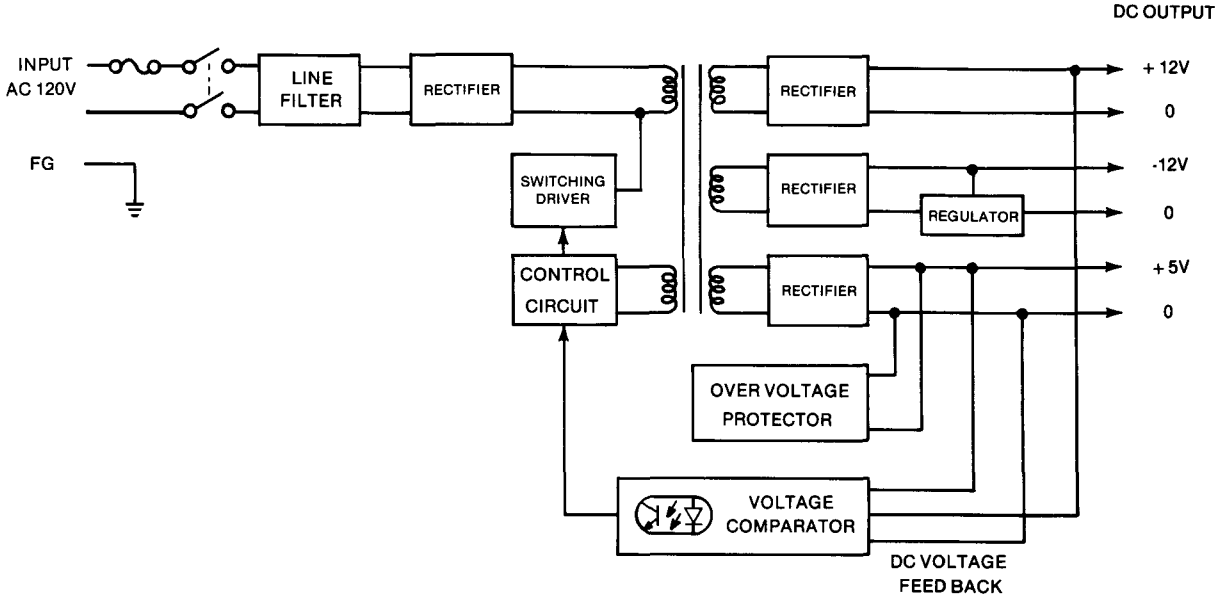
1000 EX 28 WATT SINGLE INPUT POWER SUPPLY
CONTENTS

OPERATING CHARACTERISTICS
BLOCK DIAGRAM
THEORY OF OPERATION
TROUBLESHOOTING
PARTS LIST
PCB ART
SCHEMATIC

OPERATING CHARACTERISTICS

	MINIMUM	TYPICAL	MAXIMUM	UNITS
Operating Voltage Range	90	120	135	VAC
Line Frequency	47	50/60	63	Hz
Output Voltage				
Vo1	4.85	5.00	5.15	V
Vo2	11.40	12.00	12.60	V
Vo3	-13.20	-12.00	-10.80	V
Output Loads				
Io1	1.25	-	3.0	A
Io2	0.1	-	1.25	A
Io3	0	-	0.1	A
Over Current Protection				
Current Limit ICL1	-	-	6.0	A
ICL2	-	-	2.5	A
ICL3	-	-	1.0	A
Over Voltage Protection				
Crowbar	5.8	-	6.8	V
Output Noise				
Vo1	-	-	50	mV P-P
Vo2	-	-	100	mV P-P
Vo3	-	-	150	mV P-P
Efficiency	65	69	-	%
Holdup Time				
Full Load at Nominal Line	16	-	-	mSec
Insulation Resistance				
Input to Output	7	1000	-	M ohms
Input to Ground	7	1000	-	M ohms
Isolation				
Input to Ground	1.7	-	-	KVDC

Power Supply Block Diagram



Theory of Operation

AC Input Circuit

This circuit is composed of an AC Power Switch, a fuse, a line filter, and an inrush current limiting circuit and rectifying smoothing circuit. The inrush current limiting circuit controls the charging current to electrolytic capacitors when power is ON. The line filter reduces noise that leaks from the power source to the AC line or that returns from the unit to the power souce; it satisfies the specifications of noise regulations.

Control Circuit & Power Converter Circuit

This circuit is a self oscillation switching system, generally called an R.C.C. (Ringing Choke Converter). The R.C.C. circuit does not fix the oscillating frequency. Whenever input voltage is high or the load becomes light, the oscillating frequency will be high.

The current through R2 supplies transistor Q1's base, then Q1 turns ON. When transistor Q1 is On, the Q1 current excites the transformer T1 and voltage rises in the bias coil of T1(5-6) which leads transistor Q1 positive bias, then transistor Q1 turns ON.

When transistor Q1 turns ON, collector current charges the energy to primary inductance of transformer T1 (1-3). Increasing the collector current of transistor Q1 to the point of:

$I_C > I_B .hfe$

Then, transistor Q1 immediately turns OFF. In a moment, transformer T1 will have negative voltage which will be supplied to the secondary circuit through a rectifier. A Short Circuit Protector is provided to protect transistor Q1 from excess amounts of current when the secondary circuit becomes shorted. When transistor Q2 detects the voltage drop at R8, the collector of Q2 shorts the base and emitter of Q1. Then Q1 stops working so that the circuit protects Q1 from over current.

The over current protector in the -12V line is provided by the three terminal positive voltage regulator IC1 (built-in current fold back protection), which protects Q1 against excessive current from the -12V line.

5V Output Voltage Detecting Circuit

The circuit detects the change of output load current comparing with the output voltage and AC line input voltage, which feeds back to the control circuit through a photo coupler to keep the output voltage stable. The Photo coupler isolates the primary and secondary circuits.

Over-Voltage Protection

When the +5 output voltage rises, between 5.8V to 6.8V, the +12V circuit will be shorted by the Thyristor SCR1 under the control of zener diode D12, and then the supply shuts down because of the over current protection. In the above case, correct the cause of the failure, and reinput the power. The overvoltage protection circuit will reset automatically under good conditions.

Troubleshooting

Equipment for Test Set-Up

***Isolation Transformer**(minimum of 500 VA rating)

CAUTION

Dangerously high voltages are present in this power supply. For the safety of the individual doing the testing, please use an isolation transformer. The 500 VA rating is needed to keep the AC waveform from being clipped off at the peaks. These power supplies have peak charging capacitors and draw full power at the peak of the AC waveform.

***0-140V Variable Transformer (Variac)**- Used to vary input voltage. Recommend 10 amp, 1.4 KVA rating, minimum.

***Voltmeter**- Need to measure DC voltages to 50 VDC and AC voltages to 200 VAC. Recommend two digital multimeters.

***Oscilloscope**- Need x 10 and x 100 probes.

***Load board with connectors**- See Table 1 for values of loads required. The entry on the table for Safe Load Power is the minimum power ratings for the load resistors used.

NOTE: Because of its design, this power supply must have a load present or damaging oscillations may result. Never test the power supply without a suitable load.

***Ohmmeter**

Set-Up Procedure

Set-up as shown in Figure 1. You will want to monitor the input voltage and the output voltage of the regulated bus, which is the +5 output, with DVM's. Also monitor the +5 output with the oscilloscope using 500 mv/div sensitivity. The DVM monitoring the +5 output can also be used to check the other outputs. See text of "No output" section for the test points within the power supply.

Visual Inspection

Check power supply for any broken, burned, or obviously damaged components. Visually check fuse, if any question check with ohmmeter.

Start-Up

Load power supply with minimum load as specified in Table 1. Bring up power slowly with the Variable Transformer while monitoring the +5 output with the oscilloscope and DVM. Supply should start with approximately 40-60 VAC applied, and should regulate when 90 VAC is reached. If output has reached 5 volts, do a performance test on operating characteristics, if there is no output, refer to "No output" section.

OUTPUT	MINLOAD	LOAD R	SAFE LOAD POWER	MAX LOAD	LOAD R	SAFE LOAD POWER
+5 V	1.25 A	4 ohms	20 W	3.0 A	1.7 ohms	50 W
+12 V	0.1 A	120 ohms	3 W	1.2 A	10 ohms	30 W
-12 V	0	0	0	0.1 A	120 ohms	3 W

Table 1 Load Board Values (28 watt)

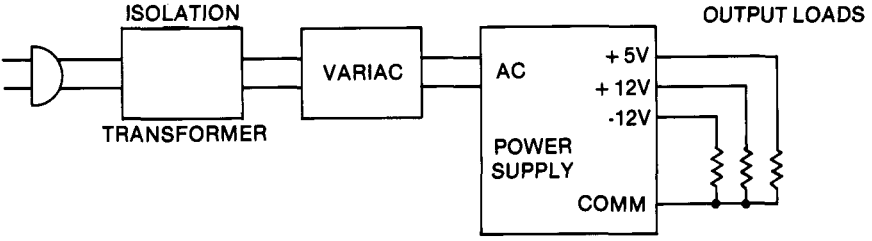


Figure 1 Test Setup

No Output

1. Check fuse:

   If fuse is blown, replace it but do not apply power until the cause of the failure is found.

2. Preliminary Check on Major Primary Components:

   Check diode bridge (D1), power transistor (Q1), and drive transistor (Q2), for shorted junctions. If any component is found shorted, replace it.

3. Preliminary Check on Major Secondary Components:

   Using an ohmmeter from an output that is common to each output and with output loads disconnected, check for shorted rectifiers or capacitors.

4. Check Over Voltage Protector:

   Read the output voltage with a DVM at the +5 output terminals by increasing the input voltage from OV. Output voltage will appear at some input voltage and then go down to OV again. Check the Diode D12 transistor (Q3) or Thyristor (SCR1).

5. Check Q1 Waveforms:

   Read waveform of Q1 Collector with oscilloscope at x 100 probe.

   Figure 2 is Q1 Collector normal waveform.

   Figure 3 is Q1 Base normal waveform.

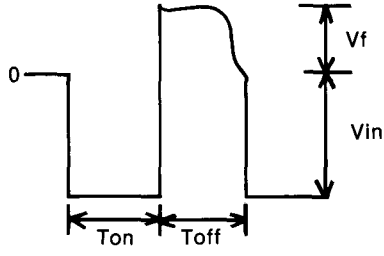
   Figure 4 is the waveforms when shorted circuits of the secondary parts as listed in Table 2. Check listed parts according to the waveform.

Collector Waveforms	Shorted Secondary Components
Figure 4	D6, D9, D10, D11, C9, C10, C11, C12, C13 C14, C15, IC1, SCR1

Table 2. List of Shorted Circuits

Waveforms

Power Converter Circuit



Collector Voltage Waveform

Collector Current Waveform

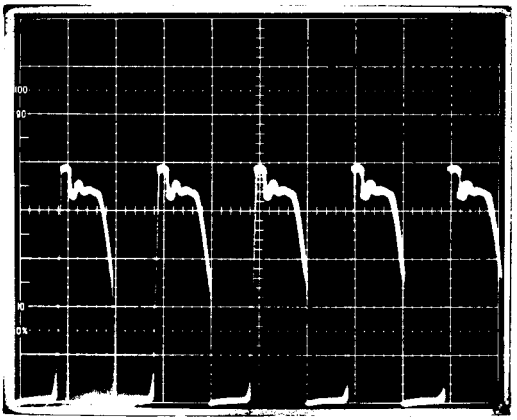
The input and output voltage are represented by the following equations:

Vo = n x Vf

Vo : Output voltage
n : Turn ratio of the transformer T1
Vf : Collector Voltage at turn-off time

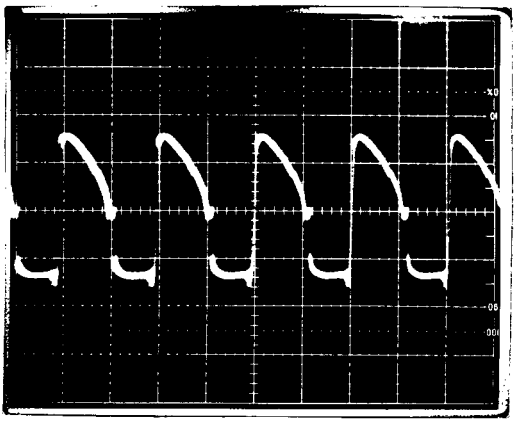
Vin x Ton = Vf x Toff

Vin : Input voltage
Ton : Turn-on time of transistor
Toff: Turn-off time of transistor



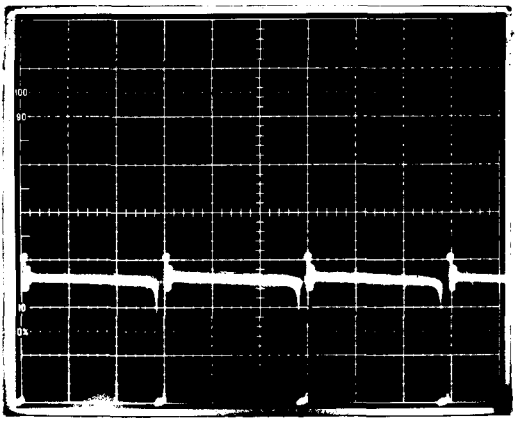
50V/DIV
5µs/DIV

Q1 Collector Waveforms (Input 90 VAC Minimum Load)



0.5V/DIV
5µs/DIV

Q1 Base Waveforms (Input 90 VAC Minimum Load)



50V/DIV
5µs/DIV

Q1 Collector Waveforms -
Shorted Secondary Components (Input 90 VAC)

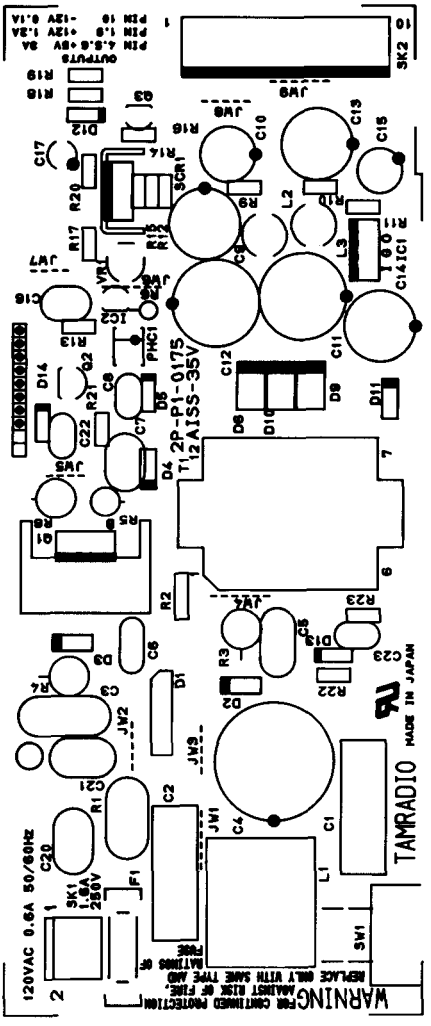
PARTS LIST FOR SWITCHING POWER SUPPLY UNIT

PART NO. 8790083

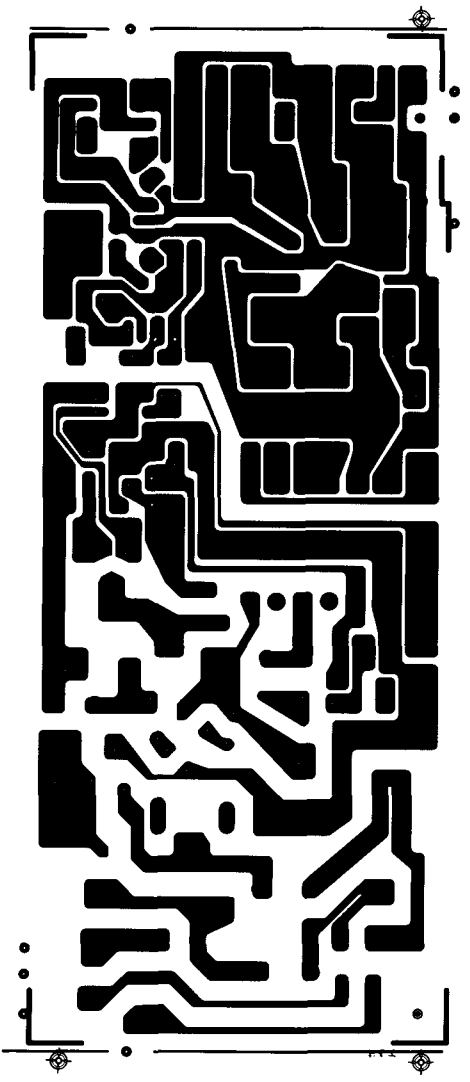
Symbol	Description			QTY	RS Part No.	Mfr's Part No.
CAPACITORS						
C1/2	Film	0.1uF	250VAC	2		XE-104
C3	Ceramic	10000pF	400VAC	1		DE7150FZ103PVA1-KC or CS17-F2GA103ZYAS
C4	Electrolytic	220uF	200WV	1		CEFTW2D221 or 200LPSS220
C5	Film	0.01uF	400VAC	1		CF921L2J103K or MDD22J103K
C6	Ceramic	680pF	2KV	1		DE1010R681K2K or CK45-B3DD681KYAR
C7/16	Film	0.1uF	50V	2		50F2D104K or AMZF104K50V
C8/22/23	Film	0.047uF	50V	3		50F2D473K or AMZF473K50V
C9/13	Electrolytic	1000uF	16WV	2		CEUSM1C102
C10	Electrolytic	470uF	16WV	1		CEUSM1C471
C11/12	Electrolytic	4700uF	10WV	2		CEUSM1A472
C14	Electrolytic	330uF	35WV	1		CEUSM1V331
C15	Electrolytic	100uF	25WV	1		CEUSM1E101
C17	Electrolytic	1uF	50WV	1		CEUSM1H010
C20/21	Ceramic	2200pF	400VAC	2		DE7100F222MVA1-KC or CS13-E2GA222MYAS
CONNECTORS						
SK1	Connector, 2 conductors Input			1		5277-02A
SK2	Connector, 10 conductors Output			1		5273-10A
DIODES						
D1	Silicon, Stack	400V	1A	1		DBA10E or SIVBA40
D2/3/4	Silicon	600V	1A	3		FI-06 or V19G
D5/13	Silicon	100V	200mA	2		DS446 or 1S954
D6	Silicon	40V	3A	1		RK44 or D3S4M
D9/10	Silicon	35V	3A	2		RK43 or D3S3M
D12	Silicon, Zener	6V	400mW	1		HZ6B2

Symbol	Description			QTY	RS Part No.	Mfr's Part No.
FUSE						
F1	Fuse	250V	1.6A	1		MT4 1.6A250V
	Fuse Clip			2		P#5722113
HEATSINK						
HS1	Heatsink, for Q1			1		4P-D2-0170
HS2	Heatsink, for SCR1			1		4P-D2-0122
INDUCTORS						
L1	Choke Coil	8mH		1		TO-9161-1 or TO-9161
L2/3	Choke Coil	5uH		2		TO-9177
INTEGRATED CIRCUITS						
IC1	IC, Regulator	12V	0.5A	1		L78M12 or NJM78M12
IC2	IC, Regulator	37V	150mA	1		TL431CLPB or uA431AWC
PHOTO COUPLERS						
PHC1	Photo Coupler	35V	50mA	1		TLP521-1 or PC817
PRINTED CIRCUIT BOARD						
PC1	Printed Circuit Board 105°C		XPC	1		2P-P1-0175
RESISTORS						
R1	Thermister	8	1.6A	1		115-080-42308 or 8D-11 or NTH9D160LA
R2	Carbon	100K	1/2W	1		RD50P100KohmsJ or RD50S100KohmsJ
R3	Metal-oxide	27	2W	1		RSF2B27ohmsJ or ERG2ANJ270
R4	Metal-oxide	100	2W	1		RSF2B100ohmsJ or ERG2ANJ101
R5	Metal-oxide	56 (27-82)	2W	1		RSF2B56ohmsJ or ERG2ANJ560 (Adjust 27-82ohms/270-820)
R6/9/10/11/16/20	Carbon	1K	1/4W	6		RD25P1KohmsJ or RD25S1KohmsJ

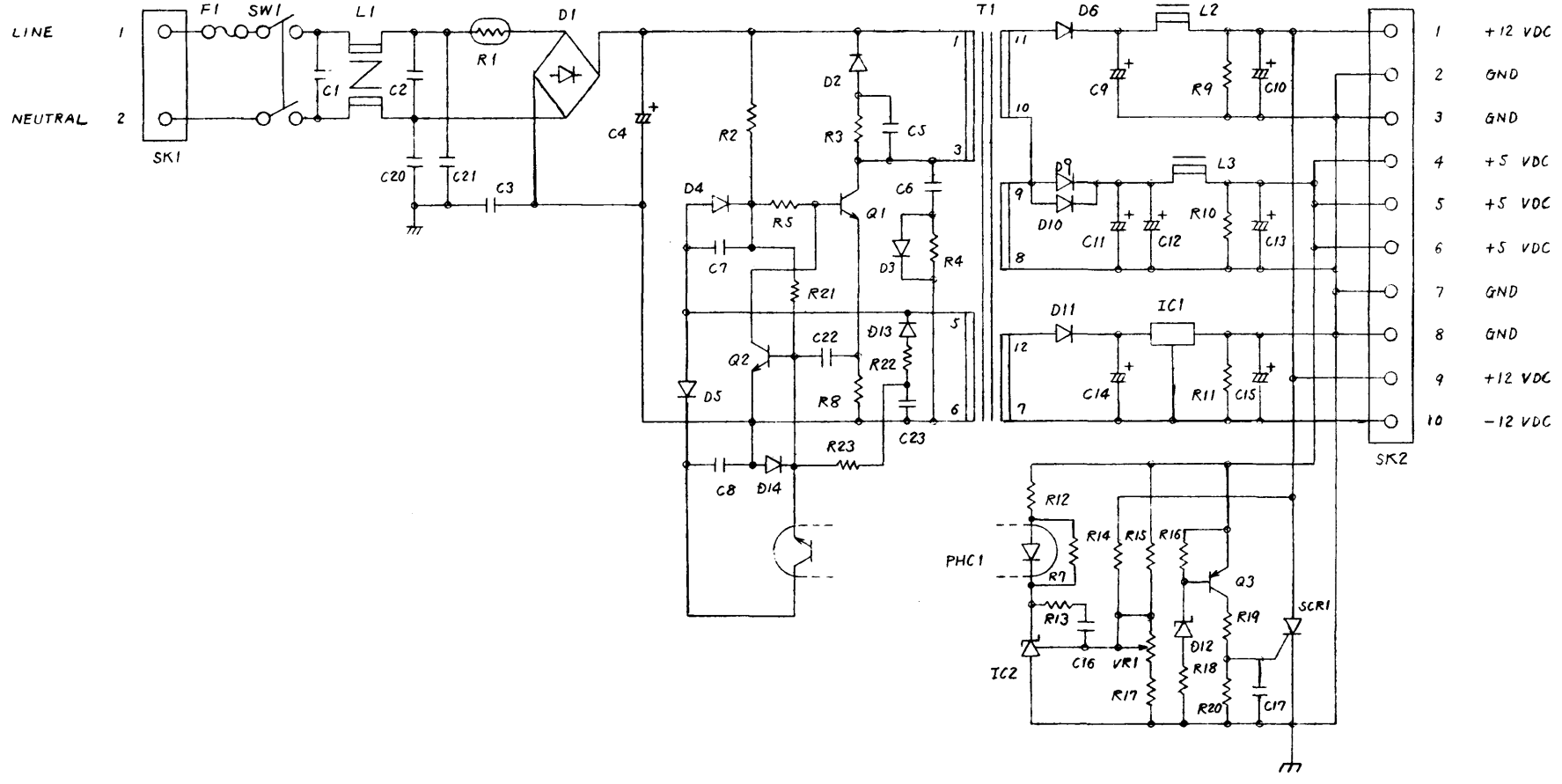
Symbol		Description		QTY	RS Part No.	Mfr's Part No.
R8	Carbon	0.68	3W	1		SPR3B
R12/22	Carbon	100	1/4W	2		RD25P100ohmsJ or RD25S100ohmsJ
R13/17	Carbon	2.2K	1/4W	2		RD25P2.2KohmsJ or RD25S2.2KohmsJ
R14	Carbon	27K	1/4W	1		RD25P27KohmsJ or RD25S27KohmsJ
R15	Carbon	6.8K	1/4W	1		RD25P6.8KohmsJ or RD25S6.8KohmsJ
R18	Carbon	39	1/4W	1		RD25P39ohmsJ or RD25S39ohmsJ
R19	Carbon	120	1/4W	1		RD25P120ohmsJ or RD25S120ohmsJ
R21	Carbon	470 (220-680)	1/4W	1		RD25P470ohmsJ or RD25S470ohmsJ (Adjust 220-680ohms)
R23	Carbon	330 (220-680)	1/4W	1		RD25P330ohmsJ or RD25S330ohmsJ (Adjust 220-680ohms)
VR1	Variable Resistor	2K	0.5W	1		V6EK-PVC(1S)202B or H0615-222B
SWITCH						
SW1	Power	125V 6A/250V 4A		1		1852.5103
TRANSFORMER						
T1	Transformer			1		TO-4349
TRANSISTORS						
Q1	Transistor	400V	7A	1		2SC3039 or 2SC3832 or 2SC2827
Q2	Transistor	50V	2A	1		2SD1207 or 2SC2655
Q3	Transistor	50V	0.2A	1		2SA1318 or 2SA1015
SCR1	Thyristor	400V	5A	1		DRS5E or 5P4M or CR6AM8



Power Supply PCB - Silkscreen



Power Supply PCB - Component Side



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TAMURA SEISAKUSHO CO., LTD.

1000 EX 28 Watt Dual Input Power Supply

1000 EX 28 WATT DUAL INPUT POWER SUPPLY
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OPERATING CHARACTERISTICS
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PCB ART
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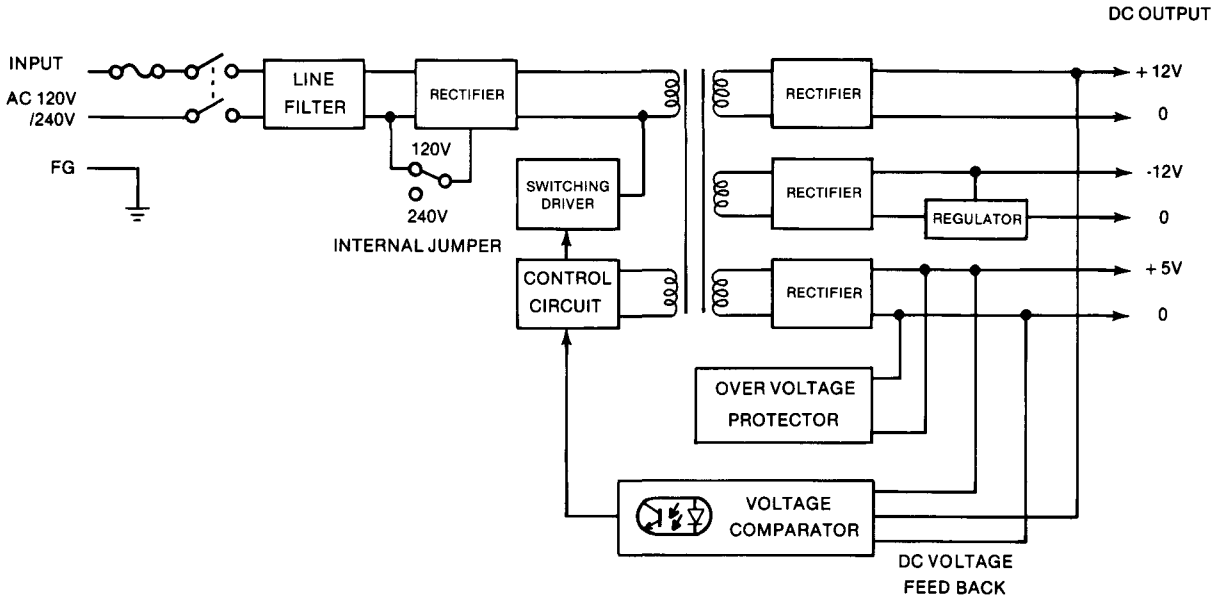
OPERATING CHARACTERISTICS

	MINIMUM	TYPICAL	MAXIMUM	UNITS
Operating Voltage Range	90 198	120 240	135 264	VAC
Line Frequency	47	50/60	63	Hz
Output Voltages				
Vol	4.85	5.00	5.15	V
Vo2	11.40	12.00	12.60	V
Vo3	-13.20	-12.00	-10.80	V
Output Loads				
Iol	1.25	-	3.0	A
Io2	0.1	-	1.25	A
Io3	0	-	0.1	A
Over Current Protection				
Current Limit ICL1	-	-	6.0	A
ICL2	-	-	2.5	A
ICL3	-	-	1.0	A
Over Voltage Protection				
Crowbar	5.8	-	6.8	V
Output Noise				
Vol	-	-	50	mV P-P
Vo2	-	-	100	mV P-P
Vo3	-	-	150	mV P-P
Efficiency	65	69	-	%
Holdup Time				
Full Load at Nominal Line	16	-	-	mSec
Insulation Resistance				
Input to Output	7	1000	-	M ohms
Input to Ground	7	1000	-	M ohms
Isolation				
Input to Ground	1.25	-	-	KVAC
Input to Output	3.75	-	-	KVAC



POWER SUPPLY BLOCK DIAGRAM

Theory of Operation

AC Input Circuit

This circuit is composed of an AC Power Switch, a fuse, a line filter, and an inrush current limiting circuit and rectifying smoothing circuit. The inrush current limiting circuit controls the charging current to electrolytic capacitors when power is ON. The line filter reduces noise that leaks from the power source to the AC line or that returns from the unit to the power souce; it satisfies the specifications of noise regulations.

Control Circuit & Power Converter Circuit

This circuit is a self oscillation switching system, generally called an R.C.C. (Ringing Choke Converter). The R.C.C. circuit does not fix the oscillating frequency. Whenever input voltage is high or the load becomes light, the oscillating frequency will be high.

The current through R3 supplies transistor Q1's base, then Q1 turns ON. When transistor Q1 is On, the Q1 current excites the transformer T1 and voltage rises in the bias coil of T1(5-6) which leads transistor Q1 positive bias, then transistor Q1 turns ON.

When transistor Q1 turns ON, collector current charges the energy to primary inductance of transformer T1 (1-3). Increasing the collector current of transistor Q1 to the point of:

$I_C = I_B .h_{fe}$

Then, transistor Q1 immediately turns OFF. In a moment, transformer T1 will have negative voltage which will be supplied to the secondary circuit through a rectifier. A Short Circuit Protector is provided to protect transistor Q1 from excess amounts of current when the secondary circuit becomes shorted. When transistor Q2 detects the voltage drop at R8, the collector of Q2 shorts the base and emitter of Q1. Then Q1 stops working so that the circuit protects Q1 from over current.

The over current protector in the -12V line is provided by the three terminal positive voltage regulator IC1 (built-in current fold back protection), which protects Q1 against excessive current from the -12V line.

5V Output Voltage Detecting Circuit

The circuit detects the change of output load current compared with the output voltage and AC line input voltage, which feeds back to the control circuit through a photo coupler to keep the output voltage stable. The Photo coupler isolates the primary and secondary circuits.

Over-Voltage Protection

When the +5 output voltage rises, between 5.8V to 6.8V, the +12V circuit will be shorted by the Thyristor SCR1 under the control of zener diode D14, and then the supply shuts down because of the over current protection. In the above case, correct the cause of the failure, and reinput the power. The overvoltage protection circuit will reset automatically under good conditions.

Troubleshooting

Equipment for Test Set-Up

***Isolation Transformer**(minimum of 500 VA rating)

CAUTION

Dangerously high voltages are present in this power supply. For the safety of the individual doing the testing, please use an isolation transformer. The 500 VA rating is needed to keep the AC waveform from being clipped off at the peaks. These power supplies have peak charging capacitors and draw full power at the peak of the AC waveform.

***0-280V Variable Transformer (Variac)**- Used to vary input voltage. Recommend 5 amp, 1.4 KVA rating, minimum.

***Voltmeter**- Need to measure DC voltages to 50 VDC and AC voltages to 300 VAC. Recommend two digital multimeters.

***Oscilloscope**- Need x 10 and x 100 probes.

***Load board with connectors**- See Table 1 for values of loads required. The entry on the table for Safe Load Power is the minimum power ratings for the load resistors used.

NOTE: Because of its design, this power supply must have a load present or damaging oscillations may result. Never test the power supply without a suitable load.

***Ohmmeter**

Set-Up Procedure

Set-up as shown in Figure 1. You will want to monitor the input voltage and the output voltage of the regulated bus, which is the +5 output, with DVM's. Also monitor the +5 output with the oscilloscope using 500 mv/div sensitivity. The DVM monitoring the +5 output can also be used to check the other outputs. See text of "No output" section for the test points within the power supply.

Table LOAD BOARD VALUES (28watt)

OUTPUT	MINLOAD	LOAD R	SAFE LOAD POWER	MAX LOAD	LOAD R	SAFE LOAD POWER
+5 V	1.25 A	4 ohms	20 W	3.0 A	1.7 ohms	50 W
+12 V	0.1 A	120 ohms	3 W	1.2 A	10 ohms	30 W
-12 V	0	0	0	0.1 A	120 ohms	3 W

Table 1 Load Board Values (28 watt)

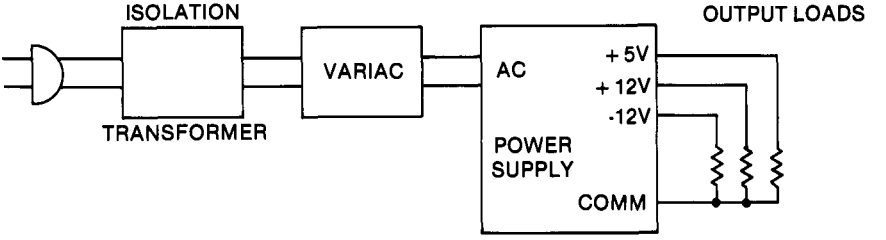


Figure 1 Test Setup

Visual Inspection

Check power supply for any broken, burned, or obviously damaged components. Visually check fuse, if any question check with ohmmeter.

Start-Up

Load power supply with minimum load as specified in Table 1. Check the voltage selector jumper and don't apply over voltage. Bring up power slowly with the Variable Transformer while monitoring the +5 output with the oscilloscope and DVM. Supply should start with approximately 40-60/80-120 VAC applied, and should regulate when 90/180 VAC is reached. If output has reached 5 volts, do a performance test on operating characteristics, if there is no output, refer to "No output" section.

No Output

1. Check fuse:

   If fuse is blown, replace it but do not apply power until the cause of the failure is found.

2. Preliminary Check on Major Primary Components:

   Check diode bridge (D1), power transistor (Q1), and drive transistor (Q2), for shorted junctions. If any component is found shorted, replace it.

3. Preliminary Check on Major Secondary Components:

   Using an ohmmeter from an output that is common to each output and with output loads disconnected, check for shorted rectifiers or capacitors.

4. Check Over Voltage Protector:

   Read the output voltage with a DVM at the +5 output terminals by increasing the input voltage from OV. Output voltage will appear at some input voltage and then go down to OV again. Check the Diode D14 transistor (Q3) or Thyristor (SCR1).

5. Check Q1 Waveforms:

   Read waveform of Q1 Collector with oscilloscope at x 100 probe.

   Figure 2 is Q1 Collector normal waveform.

   Figure 3 is Q1 Base normal waveform.

   Figure 4 is the waveforms when shorted circuits of the secondary parts as listed in Table 2. Check listed parts according to the waveform.

Collector Waveforms	Shorted Secondary Components
Figure 4	D9, D11, D12, C12, C13, C14, C15, C16 SCR1

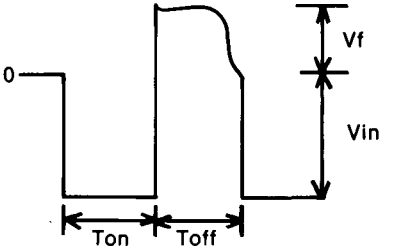
Table 2. List of Shorted Circuits

6. Check Resistor (R13).

   If R12 is open, check D13, C17 and IC1.

Waveforms

Power Converter Circuit



Collector Voltage Waveform

Collector Current Waveform

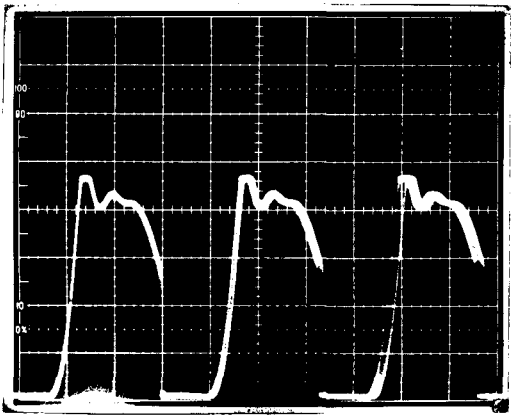
The input and output voltage are represented by the following equations:

Vo = n x Vf

Vo : Output voltage
n : Turn ratio of the transformer Tl
Vf : Collector Voltage at turn-off time

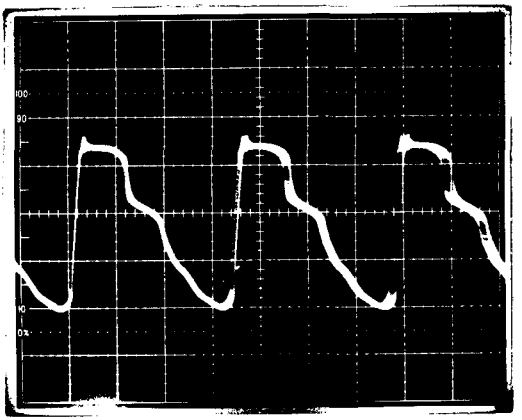
Vin x Ton = Vf x Toff

Vin : Input voltage
Ton : Turn-on time of transistor
Toff: Turn-off time of transistor



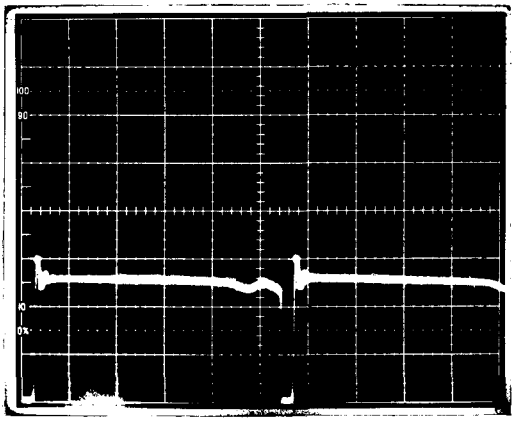
100V/DIV
5µs/DIV

Q1 Collector Waveforms (Input 90 VAC Minimum Load)



0.5V/DIV
5µs/DIV

Q1 Base Waveforms (Input 90 VAC Minimum Load)



100V/DIV
20µs/DIV

Q1 Collector Waveforms -
Shorted Secondary Components (Input 90 VAC)

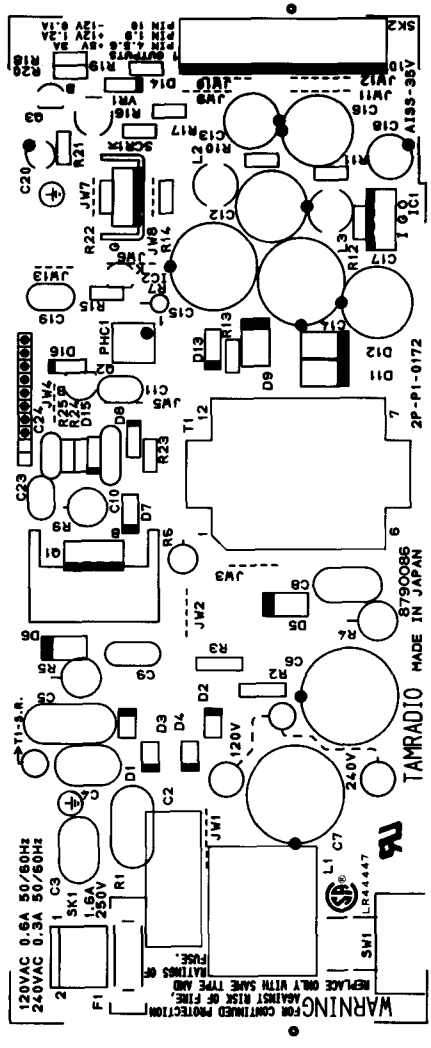
PARTS LIST FOR SWITCHING POWER SUPPLY UNIT

PART NO. 8790086

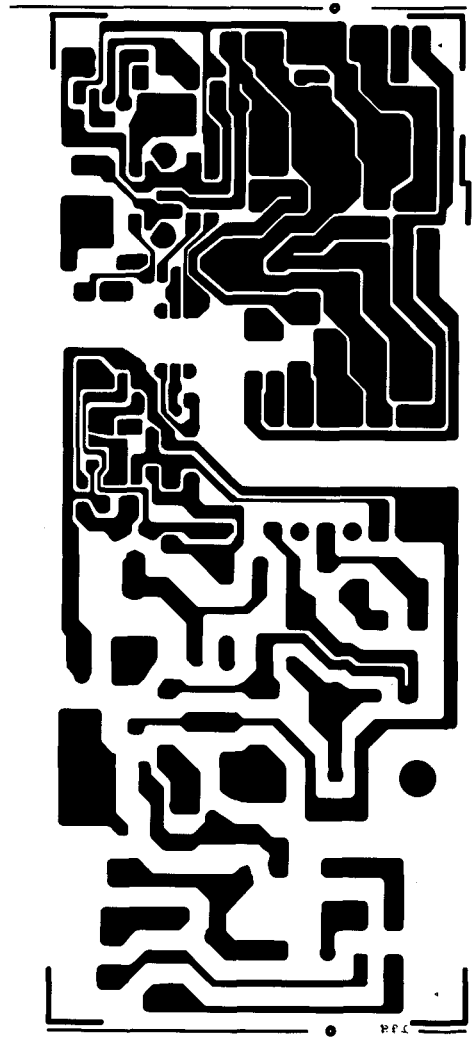
Symbol	Description			QTY	RS Part No.	Mfr's Part No.
CAPACITORS						
C2	Film	0.22uF	250VAC	1		XE-224
C3/4	Ceramic	2200pF	400VAC	2		DE7100F222MVA1-KC or CS13-E2GA222MYAS
C5	Ceramic	10000pF	400VAC	1		DE7150FZ103PVA1-KC or CS17-F2GA103ZYAS
C6/7	Electrolytic	100uF	200WV	2		CEUSM2D101
C8	Film	0.01uF	630V	1		CF921L2J103K or MDD22J103
C9	Ceramic	680pF	2KV	1		DE1010R681K2K or GK45-B3DD681KYAR
C10	Film	0.22uF (0.1-0.22uF)	50V	1		50F2D224K or AMZF224K50V (Adjust 104K-224K)
C11/23/24	Film	0.047uF	50V	3		50F2D473K or AMZF473K50V
C12/16	Electrolytic	1000uF	16WV	2		CEUSM1C102
C13	Electrolytic	470uF	16WV	1		CEUSM1C471
C14/15	Electrolytic	4700uF	10WV	2		CEUSM1A472
C17	Electrolytic	330uF	35WV	1		CEUSM1V331
C18	Electrolytic	100uF	25WV	1		CEUSM1E101
C19	Film	0.1uF	50V	1		50F2D104K or AMZF104K50V
C20	Electrolytic	1uF	50WV	1		CEUSM1H010
CONNECTORS						
SK1	Connector, 2 conductors Input			1		5277-02A
SK2	Connector, 10 conductors Output			1		5273-10A
	Pin Terminal, Voltage Selector			2		RT-01N-2.3A
	Jumping Connector			1		4P-M3-0017
DIODES						
D1/2/3/4	Silicon	600V	1A	4		DSF10G or EM01A
D5/6	Silicon	800V	1A	2		FI-08 or RU2B
D7/13	Silicon	600V	1A	2		FI-06 or V19G
D8/15	Silicon	100V	200mA	2		DS44C or 1S954
D9	Silicon	35V	3A	1		D3S4M or RK44

Symbol	Description			QTY	RS Part No.	Mfr's Part No.
D11/12	Silicon	35V	3A	2		D3S3M or RK43
D14	Silicon, Zener	6V	400mW	1		HZ6B2
FUSE						
F1	Fuse	250V	1.6A	1		MT4 1.6A250V
	Fuse Clip			2		P#5722113
HEATSINK						
HS1	Heatsink, for Q1			1		4P-D2-0170
HS2	Heatsink, for SCR1			1		4P-D2-0122
INDUCTORS						
L1	Choke Coil	40mH		1		TO-9301
L2/3	Choke Coil	5uH		2		TO-9177
INTEGRATED CIRCUITS						
IC1	IC, Regulator	12V	0.5A	1		L78M12 or NJM78M12
IC2	IC, Regulator	37V	150mA	1		TL431CLPB or uA431AWC
PHOTO COUPLERS						
PHC1	Photo Coupler	55V	60mA	1		TLP732 or PC111
PRINTED CIRCUIT BOARD						
PC1	Printed Circuit Board 105°C		XPC	1		2P-P1-0172
RESISTORS						
R1	Thermister	16	1.2A	1		16D-13 or 117-160-45202 or NTH13D160LA
R2/3	Carbon	100K	1/4W	2		RD25P100KohmsJ or RD25S100KohmsJ
R4	Metal-oxide	100K	2W	1		RSF2B100KohmsJ
R5	Metal-oxide	100	2W	1		RSF2B100ohmsJ
R6	Metal-oxide	47	2W	1		RSF2B47ohmsJ
R9	Carbon	1.2	3W	1		SPR3B1.2ohmsJ
R7/10/11/12/19/22	Carbon	1K	1/4W	6		RD25P1KohmsJ or RD25S1KohmsJ

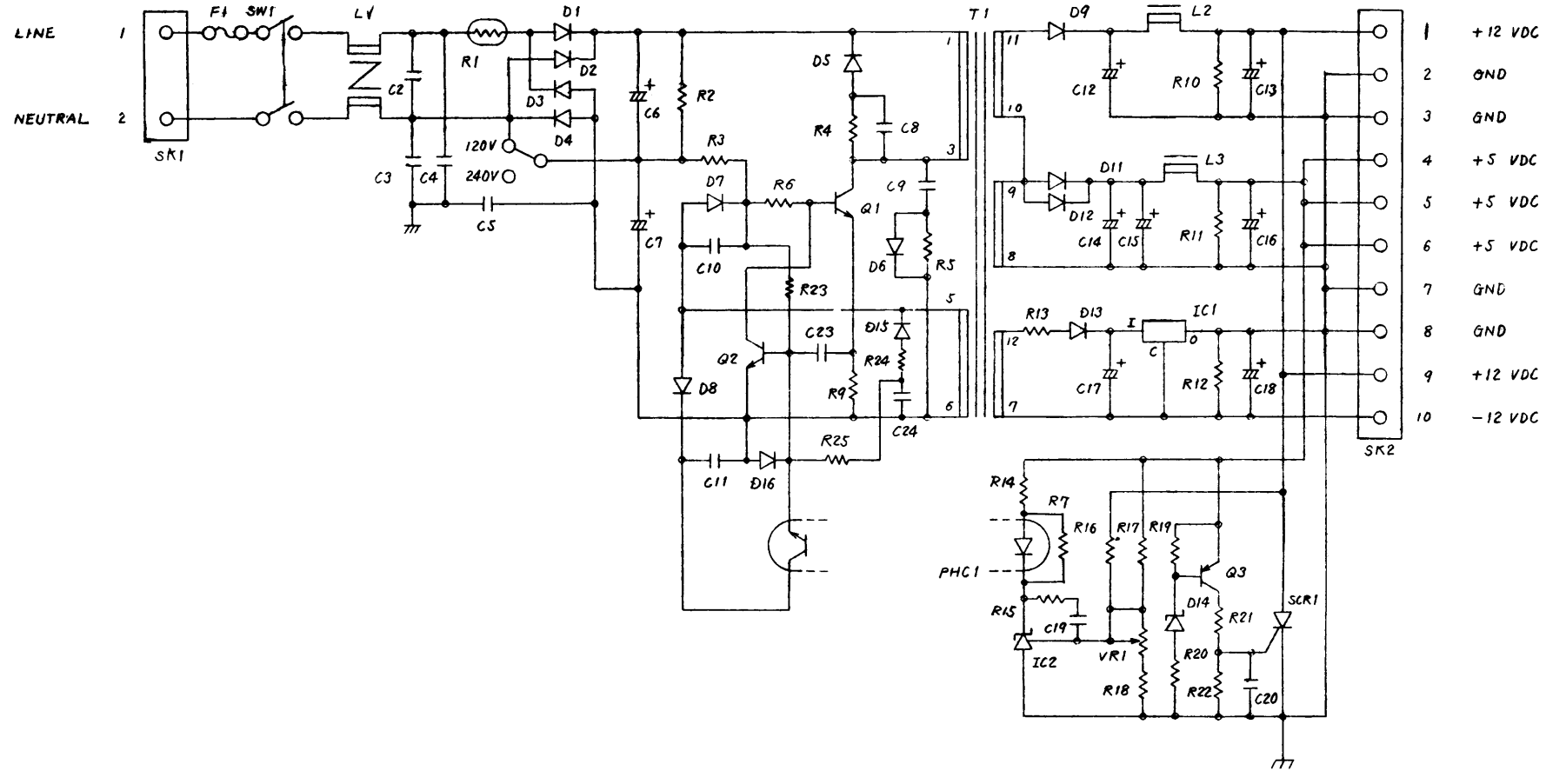
Symbol		Description		QTY	RS Part No.	Mfr's Part No.
R14	Carbon	100	1/4W	1		RD25P100ohmsJ or RD25S100ohmsJ
R15/18	Carbon	2.2K	1/4W	2		RD25P2.2KohmsJ or RD25S2.2KohmsJ
R16	Carbon	27K	1/4W	1		RD25P27KohmsJ or RD25S27KohmsJ
R17	Carbon	6.8K	1/4W	1		RD25P6.8KohmsJ or RD25S6.8KohmsJ
R20	Carbon	39	1/4W	1		RD25P39ohmsJ or RD25S39ohmsJ
R21	Carbon	120	1/4W	1		RD25P120ohmsJ or RD25S120ohmsJ
R23	Carbon	470 (330-680)	1/4W	1		RD25P470ohmsJ or RD25S470ohmsJ (Adjust 330-680ohms)
R24	Carbon	47	1/4W	1		RD25P47ohmsJ or RD25S47ohmsJ
R25	Carbon	330 (220-330)	1/4W	1		RD25P330ohmsJ or RD25S330ohmsJ (Adjust 220-330ohms)
R13	Fusing	1	1/4W	1		RF25S1ohmsJ
VR1	Variable Resistor	2K	0.5W	1		V6EK-PV(1S)202B or H0615-222B
SWITCH						
SW1	Power	125V 6A/250V 4A		1		1852.5103
TRANSFORMER						
T1	Transformer			1		TO-4338
TRANSISTORS						
Q1	Transistor	800V	3A	1		2SC3150 or 2SC4042
Q2	Transistor	50V	2A	1		2SD1207 or 2SC2655
Q3	Transistor	50V	0.2A	1		2SA1318 or 2SA1015
SCR1	Thyristor	400V	5A	1		DRA5E or SP4M or CR6AM8



Power Supply PCB - Silkscreen



Power Supply PCB - Component Side



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KEYBOARD

KEYBOARD
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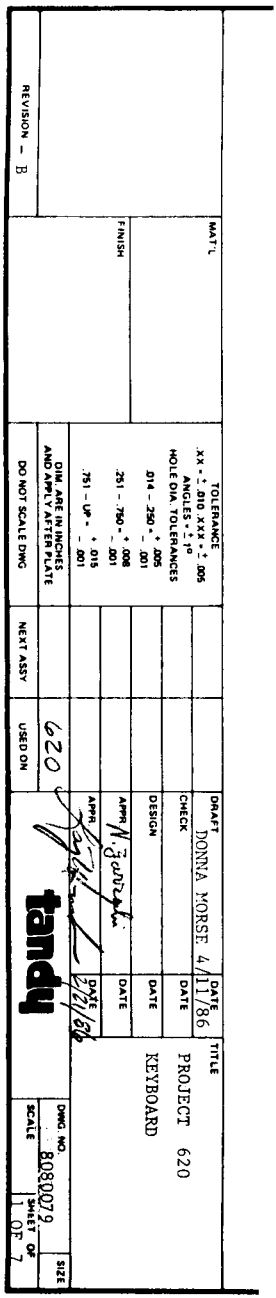


SPECIFICATION

PROJECT 620

NON-ENCODED KEYBOARD MATRIX

* REV-A 12-18-85

* REV-B 2-11-86

SEE SHEET 1A FOR REVISIONS

REV.	DESCRIPTION	DATE	APPD
C	PAGE 6: 11/5/85 REMOVED LEDS FROM KEYCAPS; DELETED NOTE OF LEDS; ADDED LED FLANGE & .150 SLOTS; .438 WAS .563; ADDED SH. 2. 11/5/85 RELEASED FOR QUOTATION ONLY 12/2/85 ADDED 3RD LED MOUNTING HOLE; MOVED J1 OFF C.L.; 5.81 WAS 5.75; ADDED SPLIT CABLE OPTION AND INCREASED OVERALL WIDTH & MOUNTING DIMS; DWG. WAS #8010010. 1/10/86 DELETED SINGLE CABLE OPTION; CHG'D 8 & 12 POSITION CABLES TO 12 & 13 POSITION CABLES, RESPECTIVELY. 2/20/86 SPACE BAR WAS CHANGED FROM 9 KEY LENGTH TO 8 KEY LENGTH. 4/11/86 ADDED PAGE 7. 4/11/86 REVISED CABLE ASSY., ADDED "J1" & "J2" DETAIL. RELEASED FOR PRODUCTION	4/11/86	
D	REVISED CABLE LENGTHS: 5.84 WAS 6.43, 6.11 WAS 6.70, 6.39 WAS 6.98, 6.63 WAS 7.22.	5/15/86	

SPECIFICATION
NON-ENCODED KEYBOARD MATRIX

1. Scope

This specification covers a keyboard.

2. Electrical Characteristics

2-1 Contact Resistance :

500 Ohm Max.,5Vdc 1mA

2-2 Contact Bounce :

10msec Max. (operating speed at 250 mm/sec)

2-3 Insulation Resistance :

50Mohm Min. at 250Vdc (between switch contacts)

2-4 Dielectric Withstand Voltage :

250 Vdc for 1 minute (betweem PCB pattern and iron panel)

150 Vdc for 1 minute (between switch contacts)

3. Mechanical Characteristics

3-1 Operating Force :

70g+/-25g at full stroke (at center of keycap)

3-2 Plunger Stroke :

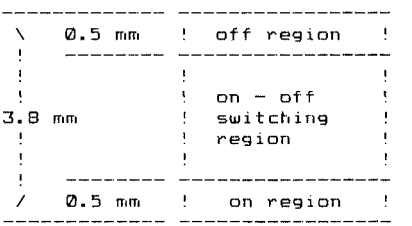
3.8mm+/-0.5

3-3 Operating Point :

0.5mm Mim. to full stroke

3-4 Release Point :

0.5mm Min. to free position



4. Operating Life *

4-1 Life :

10Meg (10 million operation)

4-2 Contact Resistance :

500ohm Max. (upto 10 million), 800ohm (after 10 million)

4-3 Contact Bounce :

10msec Max. (after 10Meg)

* Conditions

(1) 5Vdc 1mA (resistive load)

(2) Operation Speed : 5 Hz

(3) Depression Force: 200g Max. (at center of keyboard)

5. Environmental Characteristics

5-1 Operating Temperature Range :

0 to 55 degrees C

5-2 Storage temperature Range :

-10 to 65 degrees C

5-3 Humidity :

10% to 95% RH (non-condensing), 45 degrees C Max.

5-4 Altitude :

-1000ft to 10000ft

5-5 Vibration :

10 to 55 Hz 1.5mm (along each of the orthogonal axis)

5-6 Shock :

50G, 11 msec 1/2 sine wave, 3 directions each 3 times.

6. Safety Standards

Keyboard must meet; UL standard 114
, CSA SPEC: C22.2 NO.0-M1982
, CSA SPEC: C22.2 NO.154-M1983

Detailed material specification will be determinded at the approval time.

7. Keycaps

7-1 Keycaps Configuration :

Keycaps must be detachable. Keycaps are preferred to look exactly the same as they are shown on D-size drawing NO. 8080079.

7-2 Keycaps Color :

Keycaps colors are specified on the D-size drawing NO.8080079

7-3 Legends :

Legends must be in black and are printed flat on the keycaps as they appear on the D-size drawing. Two shot molding or sublimation printing is preferred.

8. Drawings

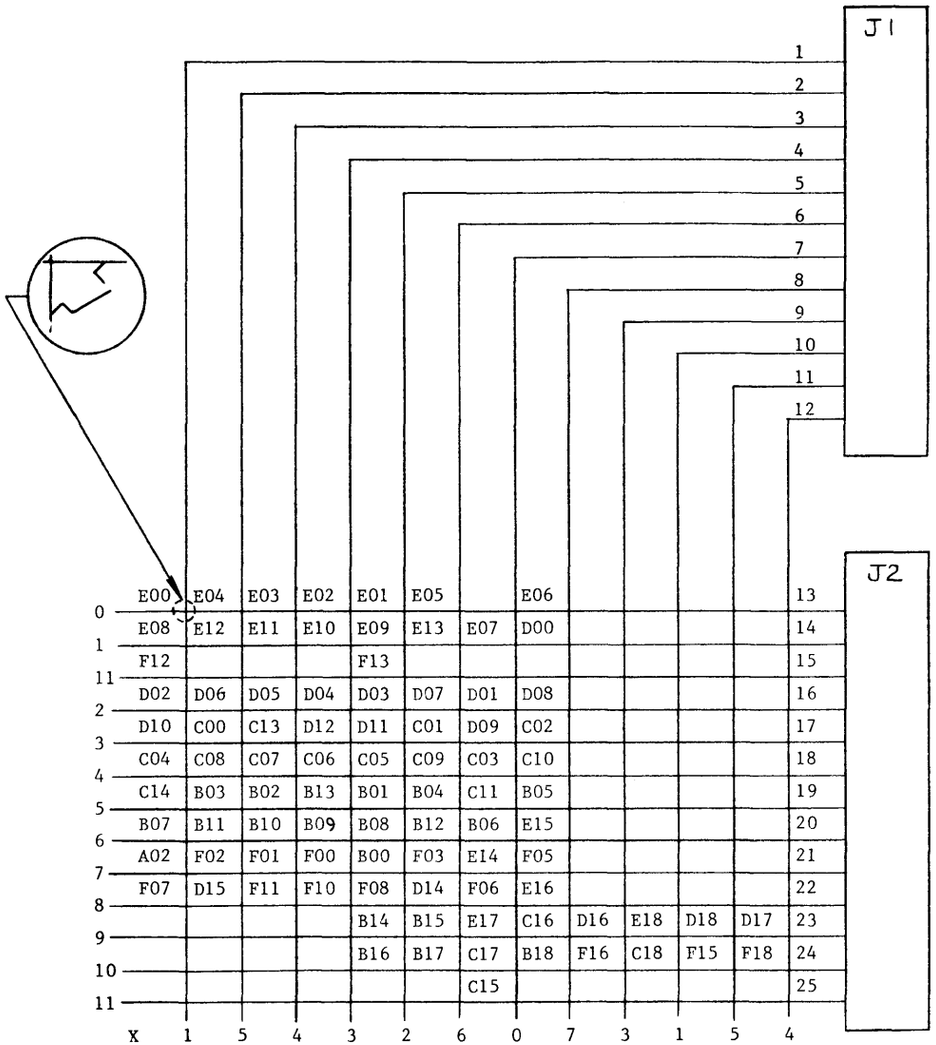
8-1 Mechanical Specifications & Keytop Arrangement :

D-8080079 Sheets 6 and 7 of 7

8-2 Circuit Specification :

B-8080079 Sheet 5 of 7

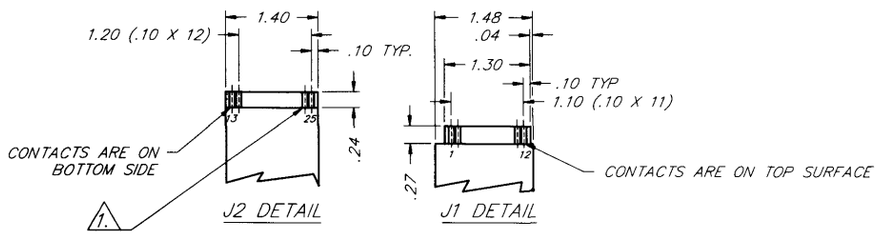
REVISION			
LTR	DESCRIPTION	DATE	APPD
—	RFQ	2-12-86	

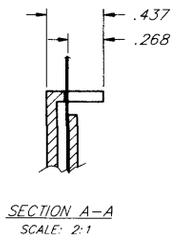


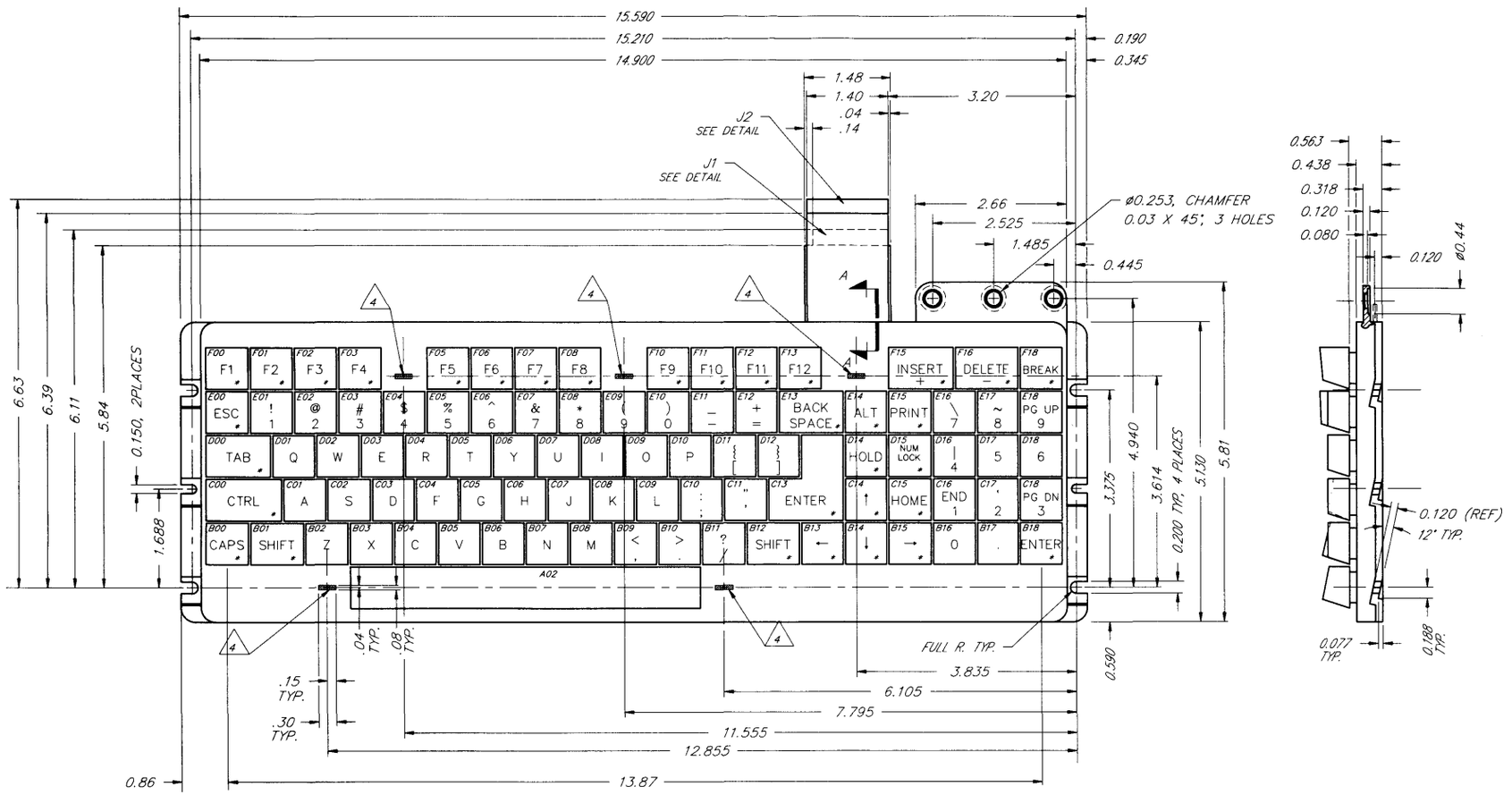
NOTES (UNLESS OTHERWISE SPECIFIED)

MAT'L	UNLESS OTHERWISE SPECIFIED		DRAFT DONNA MORSE	DATE 2-12-86	TITLE SPECIFICATION- KEYBOARD CIRCUIT PROJ. 620
	TOLERANCE .XX ± .010 XXX ± .005 ANGLES ± 1°		CHECK	DATE	
			DESIGN	DATE	
FINISH			APPD	DATE	
			APPD	DATE 4/11/86	
	DIM. ARE IN INCHES AND APPLY AFTER PLATING	620	TANDY		DWG. NO. B-8080079
	DO NOT SCALE DWG.	USED ON			SCALE NTS SHEET 5 OF 7

REVISIONS				
ZONE	LETTER	DESCRIPTION	DATE	APPROVED







4. NO SCREWS, ETC. IN THIS AREA.
3. SHEETS 1, 2, & 3 ARE "A" SIZE; SHEET 5 IS "B" SIZE.
2. KEYCAPS COLOR: ALL KEYCAPS WITH "•" IN RIGHT CORNER HAVE THE COLOR CODE: UBE CYCON AM-134914-3
   ALL OTHERS (UNMARKED) HAVE THE COLOR CODE: UBE CYCON EX 111-124369-2.
1. RIBBON CONNECTOR TRACES TO BE ON .100 CENTERS, POLARITY AS SHOWN.

NOTES:

MATERIAL	UNLESS OTHERWISE SPECIFIED		DRAFT Dan Cronch	DATE 10/4/85	TITLE	LAYOUT – KEYBOARD PROJECT 620
	TOLERANCES		CHECK Nadar Z.	DATE 4/11/86		
FINISH			DESIGN	DATE		
			APPD	DATE		
			APPD L. Hammack	DATE 4/11/86		
	DIMENSIONS ARE IN INCHES AND APPLY AFTER PLATING		TANDY		DRAWING NO.	8080079
	DO NOT SCALE THIS DRAWING	USED ON			SCALE 1:1	SHEET 6 OF 7

MEMORY PLUS

MEMORY PLUS
CONTENTS

INTRODUCTION.....1
BLOCK DIAGRAM.....1
TIMING DIAGRAM.....2
PCB ART.....3
PARTS LIST.....6
SCHEMATIC

Memory PLUS Expansion Adapter

Introduction

The major functional element of the Memory PLUS Expansion Adapter is the DMA/ Memory Controller chip. A block diagram for this chip is shown in Figure 1.

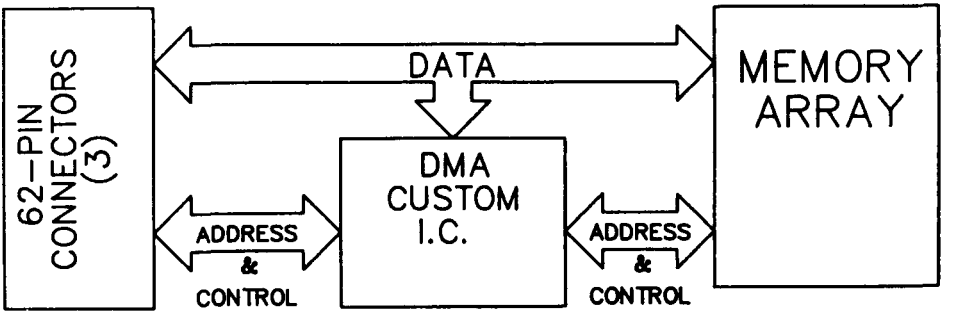


Figure 1. Memory PLUS Expansion Adapter Block Diagram

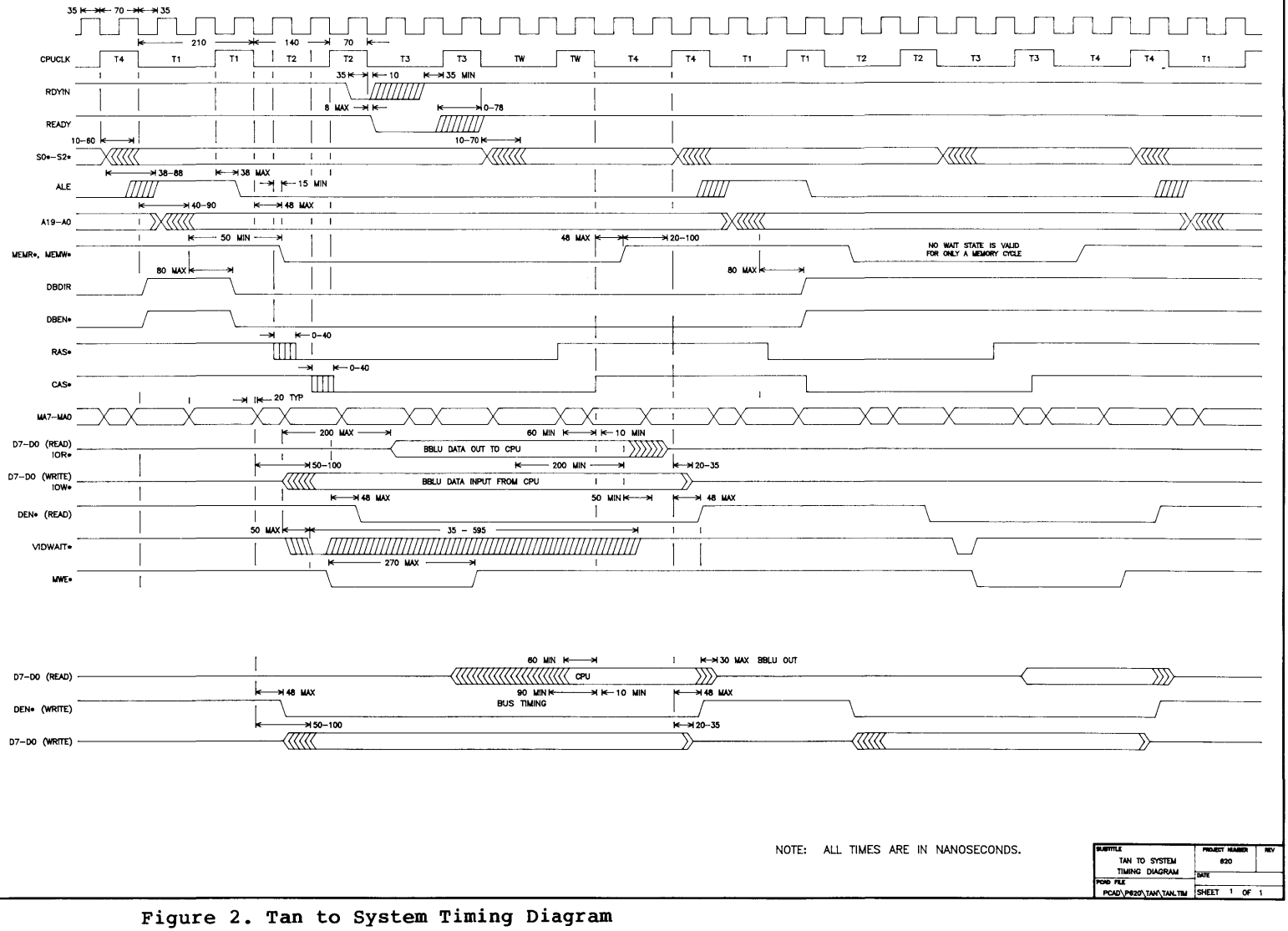
Jumper Settings

Pins E1 and E2 Must Be Jumpered Together -- if the board is going to be installed in the computer with only 128K of RAM on the Memory PLUS Expansion Adapter.

Pins E2 and E3 Must Be Jumpered Together -- if the board is going to be installed in the computer with the additional 256K of RAM on the Memory PLUS Expansion Adapter (for a total of 384K of RAM).

Theory of Operation

The custom DMA/ Memory Controller chip is composed of the equivalent of an 8237A-5 Direct Memory Access chip and a small amount of additional logic to complete the DMA function. In addition, this chip provides timing (see Figure 2.) and refresh addresses to the system memory. In the Memory PLUS Expansion Adapter, this base memory is 128K and may be expanded to 384K of memory.

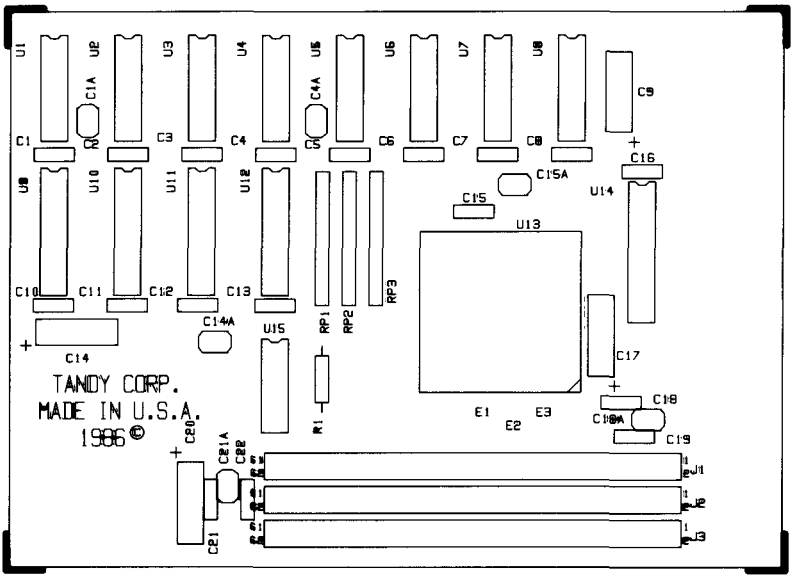


NOTE: ALL TIMES ARE IN NANOSECONDS.

SUBTITLE	PROJECT NUMBER	REV
TAN TO SYSTEM TIMING DIAGRAM	820	
PCAD FILE: PCAD\P820\TAN\TAN.TIM	DATE	SHEET 1 OF 1

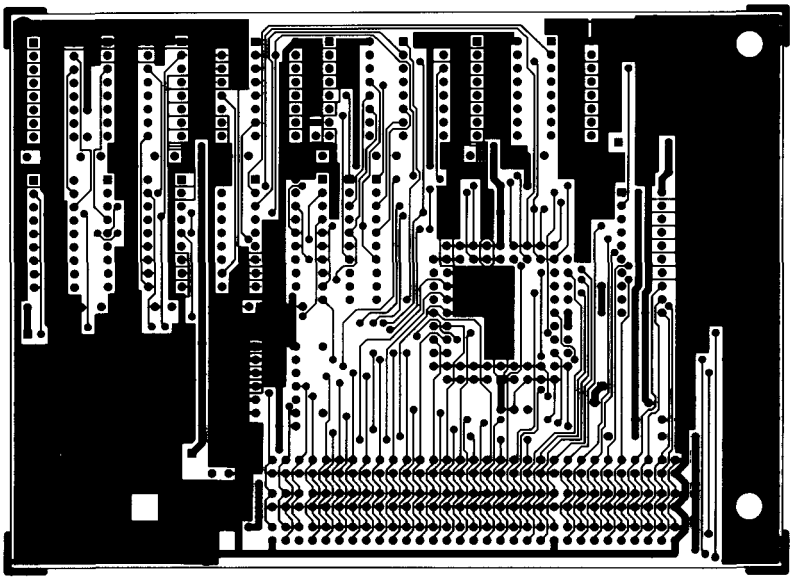
Figure 2. Tan to System Timing Diagram

TANDY SYSTEMS DESIGN FILMWORK	FAB. SPEC.: TSD-C262-0
PROJECT NO.: 804 DATE: 6/9/86	C/S SILKSCREEN
TITLE: MEMORY OPTION PCB	
DWG. NO.: 1700342 REV. A	
PART NO.: 8709701	
DESIGN GRID: x=.025 y=.025	
DESIGNER: VH DD	
INSP:	



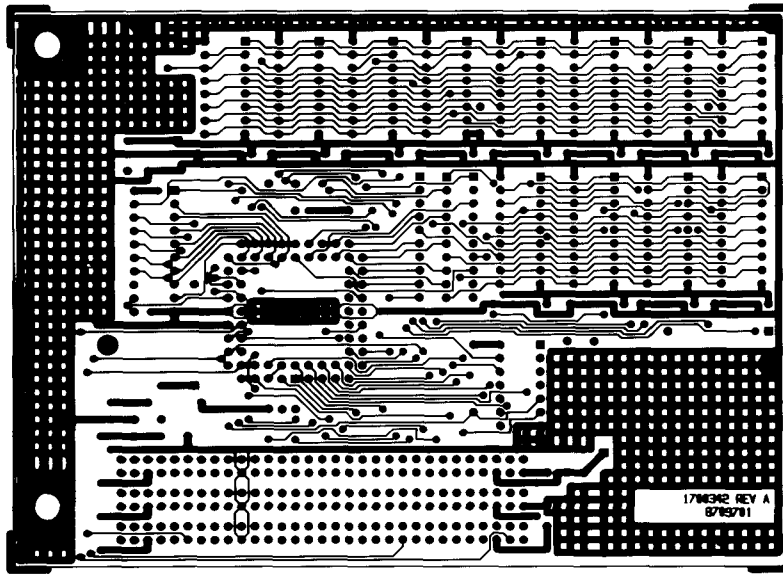
Memory PLUS Expansion Adapter - Silkscreen

TANDY SYSTEMS DESIGN FILMWORK	FAB. SPEC.: TSD-C262-0
PROJECT NO.: 804 DATE: 6/9/86	
TITLE: MEMORY OPTION PCB	
DWG. NO.: 1700342 REV. A	
PART NO.: 870970!	LAYER 1 COMPONENT SIDE
DESIGN GRID: x=.025 y=.025	
DESIGNER: VH DD	
INSP:	



Memory PLUS Expansion Adapter - Component Side

TANDY SYSTEMS DESIGN FILMWORK	FAB. SPEC.: TSD-C262-0
PROJECT NO.: 004 DATE: 6/9/86	LAYER 2 SOLDER SIDE
TITLE: MEMORY OPTION PCB	
DWG. NO.: 1700342 REV. A	
PART NO.: 8709701	
DESIGN GRID: x=.025 y=.025	
DESIGNER: VH DD	
INSP	

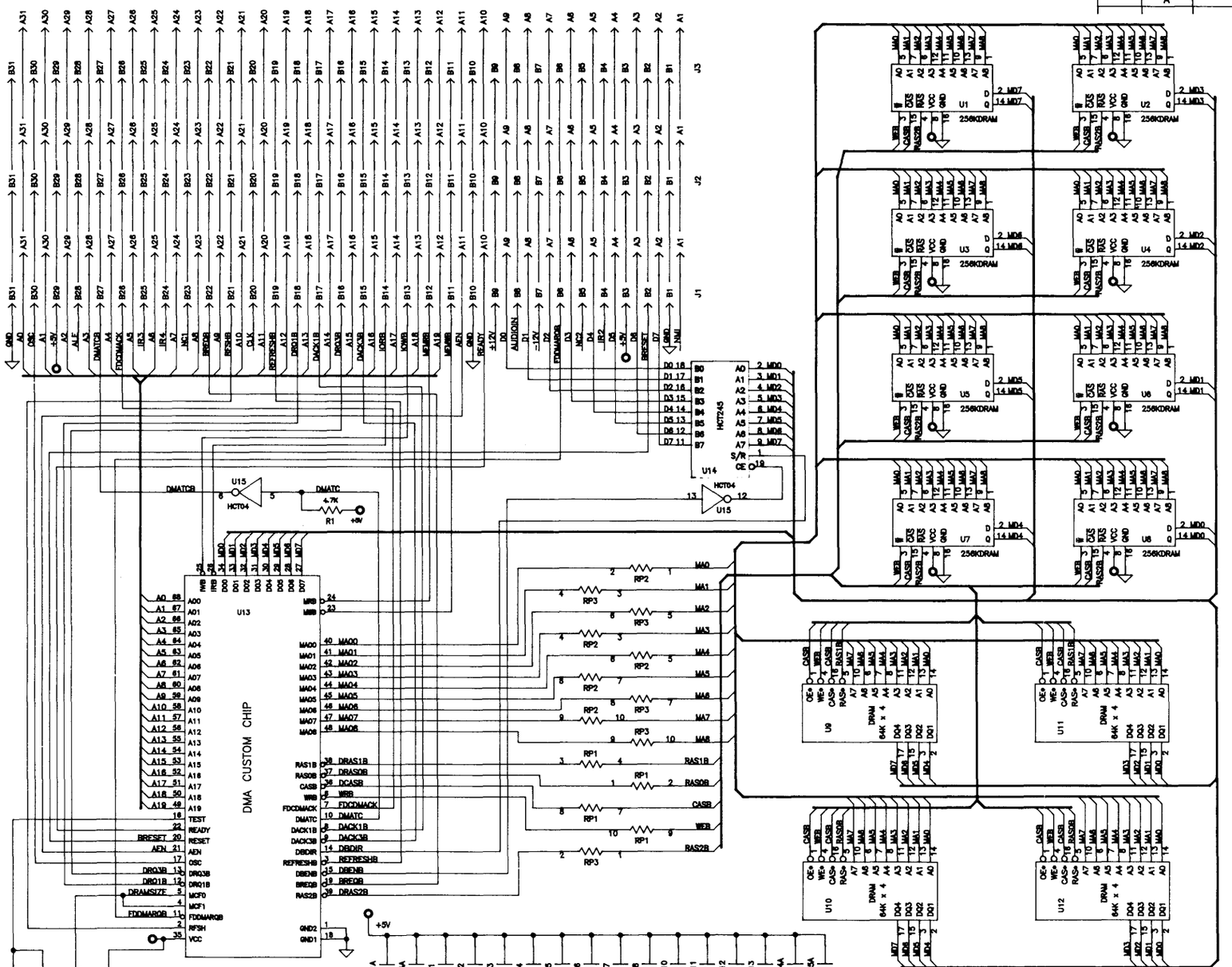


Memory PLUS Expansion Adapter - Solder Side

Memory PLUS Expansion Adapter Parts List

Symbol	Description	Number
T1000 EX Memory	Option PCB (5.75 X 4.1)	8859004
C1-8	Capacitor.33 UF 50V Mono Ax.	8374334
C1A,4A,14A,15A, 18A,21A	Capacitor 1000 PF C. Disk 50V 10% Z5P	8302104
C9,14,17,20	Capacitor 10 MF 16V Elect. Ax.	8316101
C10-13,15,16, 18,19,21,22	Capacitor.1 UF 50V Mono Ax.	8374104
E1-3	Staking Pin	8529014
J1	Connector w/Shroud (short) .687" HT. 2 X 31	8519290
J2	Connector, 2 X 31	8519257
J3	Connector (tall) 1.370" Ht. 2 X 31 with Shroud	8519312
R1	Resistor, 4.7K Ohm, 1/4W, 5%	8207247
RP1-3	Resistor Pak 33 Ohm 10-Pin 5R SIP	8290057
U1-8	IC 256K DRAM 150 NS	8049008
U1-8	Socket 16-Pin DIP	8509003
U9-12	IC 64K X 4 DRAM 150 NS	8041254
U9-12	Socket 18-Pin DIP	8509006
U13	IC DMA Custom	8075711
U13	Socket 68-Pin Jedec "C"	8509020
U14	IC 74HCT245	8026245
U15	IC 74HCT04	8026004
	Jumper Plug	8519098

ZONE	LETTER	REVISION DESCRIPTION	DATE	APPROVED
	A	PRODUCTION RELEASED		



SUBTITLE	DWG NO	REV
DMA MEMORY OPTION CARD	D-8000275	A
	SCALE	SHEET 1 OF 1

Tandy® 1000 RS-232 Interface Board

CONTENTS PAGE NO.

1/ Introduction.....1

2/ Jumper Configuration.....3
Domestic.....3
International.....4

3/ Theory of Operation.....7
Block Diagram of RS-232 Adapter (Figure 1.).....8
82S153 Pin Functions (Figure 2.).....9
82S153 IFL Equations (Figure 3.).....10

4/ Troubleshooting.....11

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7/ Schematic.....19

8/ WD8250 Asynchronous Communications Element

1/ Introduction to RS-232 Interface Board

The RS-232 board is a single-channel asynchronous serial communications board. The heart of the board is the WD8250 Asynchronous Communications Element (ACE), that functions as a serial data input/output interface. It performs serial-to-parallel conversion on data characters received from a peripheral device or a modem and parallel-to-serial conversion on data characters received from the CPU.

Status information reported includes the type and condition of the ACE's transfer operations as well as any error conditions. The WD8250 includes a programmable baud rate generator that allows operation from 50 to 9600 baud. The WD8250 can be software tailored to the user's requirements. It can add and remove start bits, stop bits, and parity bits. It supports 5-,6-,7- or 8-bit characters with 1, 1 1/2, or 2 stop bits. Diagnostic capabilities provide loopback functions of transmit/receive and input/output signals.

This manual covers both domestic and international RS-232 boards. The main difference between the domestic and international boards is the jumper configuration and the programming of the receiving baud rate. This information is covered in section 2. An international parts list is also included in section 5.

Other features include:

- Full double buffering which eliminates the need for precise synchronization.
- Independent receiver clock input.
- False start bit detection.
- Line break generation and detection.
- Modem control functions: Clear To Send (CTS), Request To Send (RTS), Data Set Ready (DSR), Data Terminal Ready (DTR), Ring Indicator (RI), and Carrier Detect (CD).

2/ Jumper Configuration

Most commercially available terminal or communications programs use the primary addresses. Points E2 and E3 should be jumpered for primary operation. Points E1 and E2 should be jumpered for secondary operation.

International RS-232 Board

The RS-232 serial communications board for the Tandy 1000 has two versions. One board is a domestic version which cannot be altered and is used for domestic operations only. Domestic operations means that the board transmits and receives at the same baud rate. The other board is an international version which can be used as either a domestic board or easily modified to accommodate international operations. International operations means that the board can be programmed to transmit at one baud rate while receiving at another baud rate. This is known to be a common mode of operation in Europe. In order for the board to operate in the international mode, some jumpers on the board will have to be changed. The jumper arrangements for domestic and international operation as well as operation in the primary and secondary address spaces are as follows:

Domestic operation in the primary address (3F8-3FF) -
- Jumper E2 to E3
- Jumper E4 to E6
- Jumper E7 to E9, E8 and E10 empty

Domestic operation in the secondary address (2F8-2FF) -
- Jumper E1 to E2
- Jumper E4 to E6
- Jumper E7 to E9, E8 and E10 empty

International operation in the primary address -
- Jumper E2 to E3
- Jumper E4 to E5
- Jumper E7 to E8
- Jumper E9 to E10

International operation in the secondary address -
- Jumper E1 to E2
- Jumper E4 to E5
- Jumper E7 to E8
- Jumper E9 to E10

While the board is jumpered to the international mode of operation, the user can select between domestic and international operation. This can be done as follows:

Primary address - 3FC, or secondary address - 2FC, Bit 2. Set low for domestic operation, set high for international operation.

NOTE: This bit is low on power up and reset.

Programming the Baud Rates for International Operation

While the Board is setup for international operation, two baud rate generators will have to be programmed. One for the transmit baud rate and the other for the receive baud rate. The transmit baud rate is supplied from the internal baud rate generator on the 8250 UART and is programmed the same as before with the domestic board. The receive baud rate is supplied from an external baud rate generator and is totally independent from the programming for the internal transmit baud rate generator. This external receive baud rate generator is enabled through address 3FF (primary) or 2FF (secondary). The baud rate generator is then programmed by sending the appropriate bits via the data bus (D0-D3). Refer to the following table for selecting the various baud rates.

Frequency Options

Transmit/Receive Address				Baud Rate	Theortical	Actual	Percent	Duty Cycle	
D	C	B	A	(16X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	0.8	0.8	--	50/50	6336
0	0	0	1	75	1.2	1.2	--	50/50	4224
0	0	1	0	110	1.76	1.76	--	50/50	2880
0	0	1	1	134.5	2.152	2.1523	0.016	50/50	2355
0	1	0	0	150	2.4	2.4	--	50/50	2112
0	1	0	1	300	4.8	4.8	--	50/50	1056
0	1	1	0	600	9.6	9.6	--	50/50	528
0	1	1	1	1200	19.2	19.2	--	50/50	264
1	0	0	0	1800	28.8	28.8	--	50/50	176
1	0	0	1	2000	32.0	32.081	0.253	50/50	158
1	0	1	0	2400	38.4	38.4	--	50/50	132
1	0	1	1	3600	57.6	57.6	--	50/50	88
1	1	0	0	4800	76.8	76.8	--	50/50	66
1	1	0	1	7200	115.2	115.2	--	50/50	44
1	1	1	0	9600	153.6	153.6	--	48/52	33
1	1	1	1	19,200	307.2	316.8	3.125	50/50	16

Crystal Frequency = 5.0688 MHZ

3/ Theory Of Operation

The user's manual for the TRS-80 RS-232-C Interface (Cat. No. 26-1145) has a general discussion of the EIA RS-232-C Standard. The RS-232 asynchronous communications board has various modes of operation that can be selected by programming the WD8250 ACE. The WD8250 is programmed by selecting the I/O address (3F8 to 3FE primary, and 2FB to 2FE secondary), and writing data out to the board. Address bits A0, A1, and A2 are used to define the modes of operation by selecting the different registers to be programmed or read.

One interrupt is provided to the system from IRQ4 for primary operation, and IRQ3 for secondary operation. This interrupt is active high. Bit 3 of the modem control register must be set high in order to send interrupts to the system. When this bit is high, any interrupts allowed by the interrupt enable register will cause an interrupt.

Refer to Section 8 for the Functional Pin Definitions and Timing Diagrams for the WD8250.

Figure 1 shows the Block Diagram for the RS-232 Adapter.

Figure 2 shows the Functional Pin Definitions for the 82S153 IFL.

Figure 3 shows the IFL equations for the 82S153 IFL.

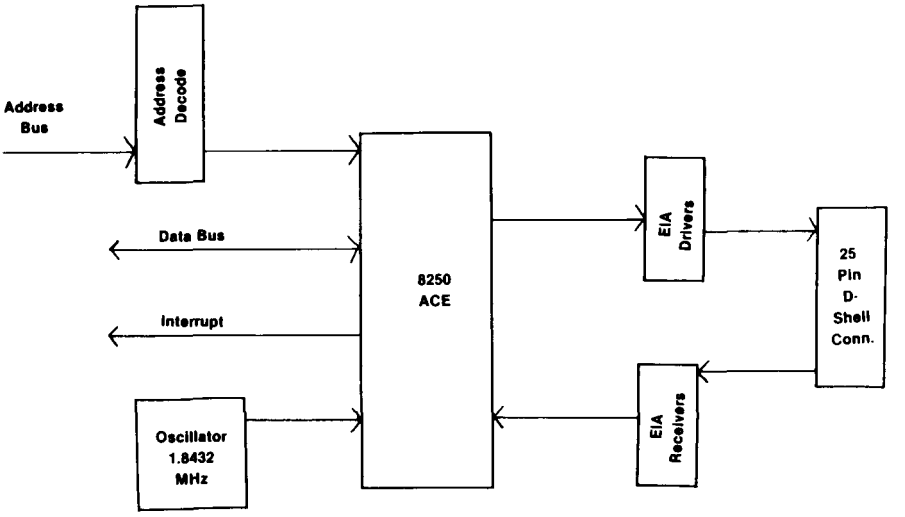


Figure 1. Block Diagram for the RS-232 Adapter.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	ADDRESS ENABLE	$\overline{AEN}$	DMA cycle when high, CPU cycle when low.
2-8	ADDRESS LINES	A3-A9	These address lines are used for decoding the address space 2F8-2FF (secondary) or 3F8-3FF (primary).
9	SECONDARY INTERRUPT REQUEST	IORQ3	Sends interrupts to the CPU while operating in the secondary address space.
10	GROUND		
11	PRIMARY INTERRUPT REQUEST	IORQ4	Sends interrupts to the CPU while operating in the primary address space.
12	PRIMARY OR SECONDARY UARTS	P or S	An input that determines which address space will be used. Primary (3F8-3FF) when high or secondary (2F8-2FF) when low.
13	UART INTERRUPT	INT	Receives interrupt signal from the 8250.
14	UART CHIP SELECT	$\overline{UCS}$	Enables the 8250 ACE when low.
15	NOT USED		
16	NOT USED		
17	DATA CHIP SELECT	$\overline{DCS}$	Enables the data bus buffers when low.
18	NOT USED		
19	NOT USED		
20	VCC		

Figure 2. Functional Pin Definitions for the 82S153 IFL.

INPUTS

PRI_PORT = IOADDRESS 3F8-3FF
SEC_PORT = IOADDRESS 2F8-2FF

OUTPUTS

$\overline{DCS}$ = PRI_PORT $\overline{AEN}$ P_OR_S + SEC_PORT AEN $\overline{P_OR_S}$

IORQ4 = MODEM_INT P_OR_S M_OR_U + UART_INT P_OR_S $\overline{M_OR_U}$

IORQ3 = UART_INT $\overline{P_OR_S}$ $\overline{M_OR_U}$ + MODEM_INT $\overline{P_OR_S}$ M_OR_U

UART_CS = PRI_PORT AEN P_OR_S + SEC_PORT AEN $\overline{P_OR_S}$

Figure 3. IFL Equations for the 82S153 IFL.

4/ Troubleshooting

The RS-232 board can be tested by using the IOTEST program included with the Tandy 1000 diagnostics diskette. The following is an excerpt from the IOTEST reference quide.

Equipment Needed

1. Computer: Tandy 1000 or 1200 HD

2. RS-232 card

3. Loopback connector test fixture in the following configuration:

DB-25	Signal
2-3	TX-RX
4-5	RTS-CTS
6-8-20-22	DTR-DSR-CD-RI

4. Tandy 1000 Diagnostic Diskette

Troubleshooting Hints

. If some of the control functions are bad:

  Check the loopback connector.
  Check the line drivers/receivers for activity.
  Check the 8250 UART (U2) for any bent pins.

. The BRG fails:

  Check for correct configuration of the jumpers.
  The 8250 UART may be malfunctioning.

. The RX test fails:

  Check for interrupts on the bus.
  Check the 8250 and jumper configurations.

- Break detect fails:

  The 8250 UART may be malfunctioning.

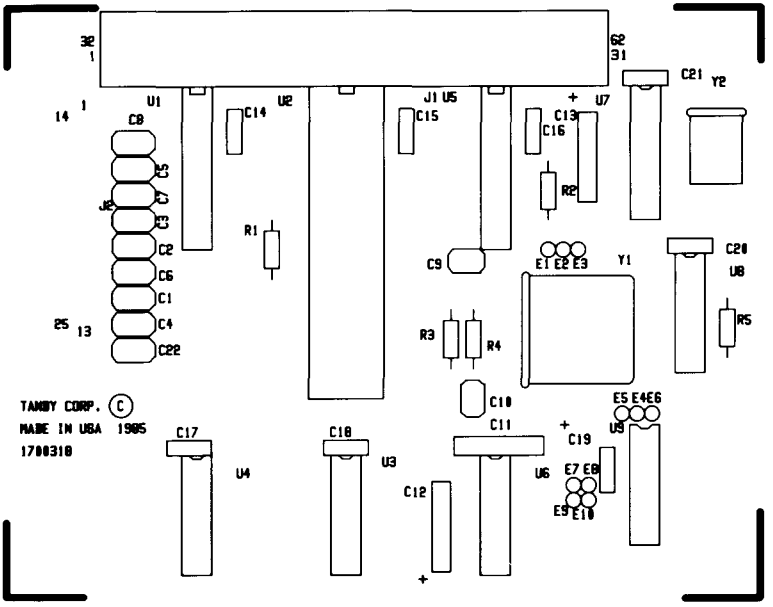
- RX and Break detect fails:

  Check the data path through the loopback connector and the line drivers/receivers.
  Check the 8250 and jumper configurations.

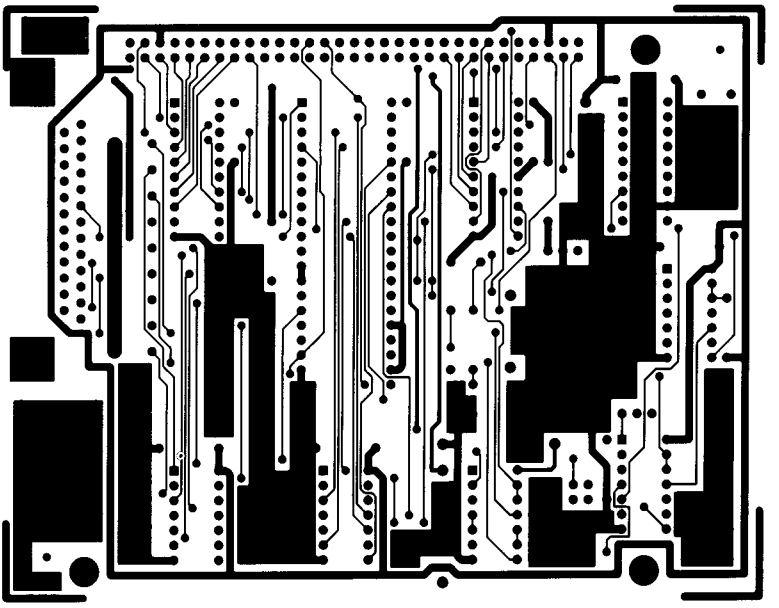
- If the above tests are negative:

  Check the 82S153 (U5).
  Check the 8250 UART and jumper configurations.
  Check the 74LS245 (U1).

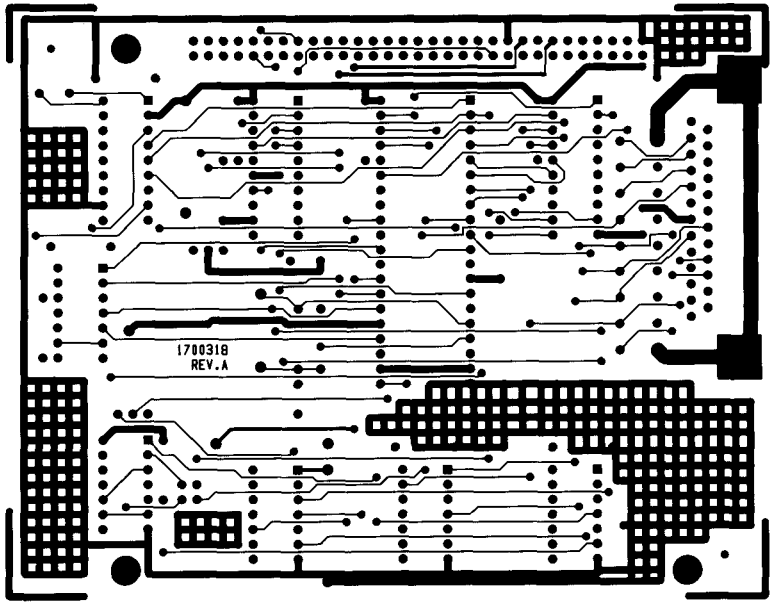
5/ Component Layout



Silkscreen



Component Side



Solder Side

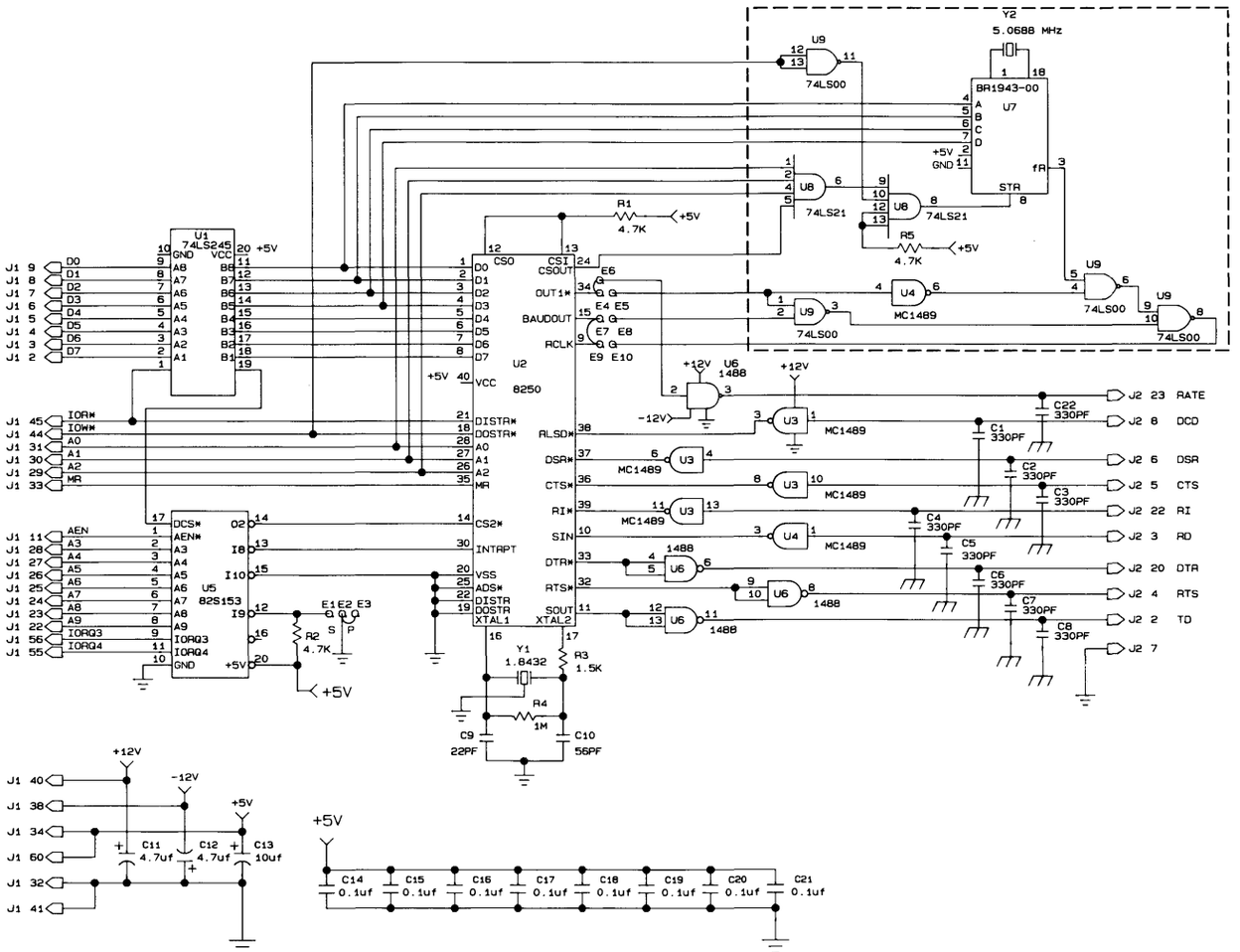
6/ Parts List
RS-232 Board
Catalog Number 25-1014

SYMBOL	QTY	DESCRIPTION	PART NO.
	1	RS-232 COMBO/ T1000 REV. A	
	3	JUMPER PLUG	AJ-6908
	3	STANDOFF	AHC-2429
	4	SCREW - 4-40 X 1/4 PAN H, MACHINE	AHD-2991
	2	NUTS - 4-40	AHD-7143
	1	PANEL BRACKET, RS-232	AHC-3192
C1-8,22	9	CAPACITOR 330 PF 5/50V C. DISK	CF-7412
C9	1	CAPACITOR 22 PF/+.5PF/50V	CC-220DJCP
C10	1	CAPACITOR 56 PF 80% 50V C. DISK	CC-560QJCP
C11-12	2	CAPACITOR 4.7 MFD 20% 50V ELEC. AXIAL	CC-475MJAA
C13	1	CAPACITOR 10 MFD +20/25V ELEC. AXIAL	CC-106MFAA
C14-18	5	CAPACITOR 0.1 MFD 50V AXIAL	CC-104JJLA
E1-10	10	STAKING PINS	AHB-9682
J1	1	RECEPTICAL	AJ-4052
J2	1	CONNECTOR, DB25 FEMALE RT. ANGLE METAL SHELL, GROUND STRAP 4-40 THREADED INSERTS	AJ-6983
R1-2	2	RESISTOR 4.7K OHM 1/4 WATT 5%	N-0247EEC
R3	1	RESISTOR 1.5K OHM 1/4 WATT 5%	N-0206EEC
R4	1	RESISTOR 1 MEG OHM 1/4 WATT 5%	N-0445EEC
U1	1	IC 74LS245 OCTAL BUS TRANSCEIVER	AMX-4470
U2	1	IC 8250 SINGLE CHIP UART	MX-6859
U2	1	SOCKET 40-PIN DIP	AJ-6580
U3-4	2	IC MC1489 RECEIVER	MX-2143
U5	1	IC 82S153 IFL, MOD UART	MX-6858
U5	1	SOCKET 20-PIN DIP	AJ-6760
U6	1	IC 1488 DRIVER	AMX-3867
Y1	1	CRYSTAL 1.8432 MHZ	MX-0097

RS-232 Board--International
Catalog Number 25-1014X

SYMBOL	QTY	DESCRIPTION	PART NO.
	1	RS-232 COMBO/ T1000 REV. A	
	4	JUMPER PLUG	AJ-6908
	3	STANDOFF	AHC-2429
	4	SCREW - 4-40 X 1/4 PAN H, MACHINE	AHD-2991
	2	NUTS - 4-40	AHD-7143
	1	PANEL BRACKET, RS-232	AHC-3192
C1-8,22	9	CAPACITOR 330 PF 5/50V C. DISK	CF-7412
C9	1	CAPACITOR 22 PF/±.5PF/ 50V	CC-220DJCP
C10	1	CAPACITOR 56 PF 80% 50V C. DISK	CC-560QJCP
C11-12	2	CAPACITOR 4.7 MFD 20% 50V ELEC. AXIAL	CC-475MJAA
C13	1	CAPACITOR 10 MFD ±20/25V ELEC. AXIAL	CC-106MFAA
C14-21	8	CAPACITOR 0.1 MFD 50V AXIAL	CC-104JJLA
E1-10	10	STAKING PINS	AHB-9682
J1	1	RECEPTICAL	AJ-4052
J2	1	CONNECTOR, DB25 FEMALE RT. ANGLE METAL SHELL, GROUND STRAP 4-40 THREADED INSERTS	AJ-6983
R1,2,5	3	RESISTOR 4.7K OHM 1/4 WATT 5%	N-0247EEC
R3	1	RESISTOR 1.5K OHM 1/4 WATT 5%	N-0206EEC
R4	1	RESISTOR 1 MEG OHM 1/4 WATT 5%	N-0445EEC
U1	1	IC 74LS245 OCTAL BUS TRANSCEIVER	AMX-4470
U2	1	IC 8250 SINGLE CHIP UART	MX-6859
U2	1	SOCKET 40-PIN DIP	AJ-6580
U3-4	2	IC MC1489 RECEIVER	MX-6859
U5	1	IC 82S153 IFL, MOD UART	MX-6858
U5	1	SOCKET 20-PIN DIP	AJ-6760
U6	1	IC 1488 DRIVER	AMX-3867
U7	1	IC BR1943-00	AMX-3921
U8	1	IC 74LS21 DUAL 4-IN AND	MX-6502
U9	1	IC 74LS00 QUAD 2-IN NAND	MX-3495
Y1	1	CRYSTAL 1.8432 MHZ	MX-0097
Y2	1	CRYSTAL 5.0688	AMX-2395

REVISION				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	—	RELEASE FOR PRODUCTION	5/22/85	



NOTES:
1. COMPONENTS WITHIN DASHED BOX USED ONLY FOR INTERNATIONAL VERSION.
2. JUMPERS SHOWN IN PRIMARY, DOMESTIC CONFIGURATION.

DRAFT	DATE	TITLE	SCHEMATIC— RS-232 COMBO TANDY 1000
CHECK	DATE		PROJECT NO. 652
DESIGN	DATE		
APPR.	DATE		
A	DATE 5/22/85		
tandy		DWG NO 8000253	SIZE D
		SCALE —	SHEET 1 OF 1

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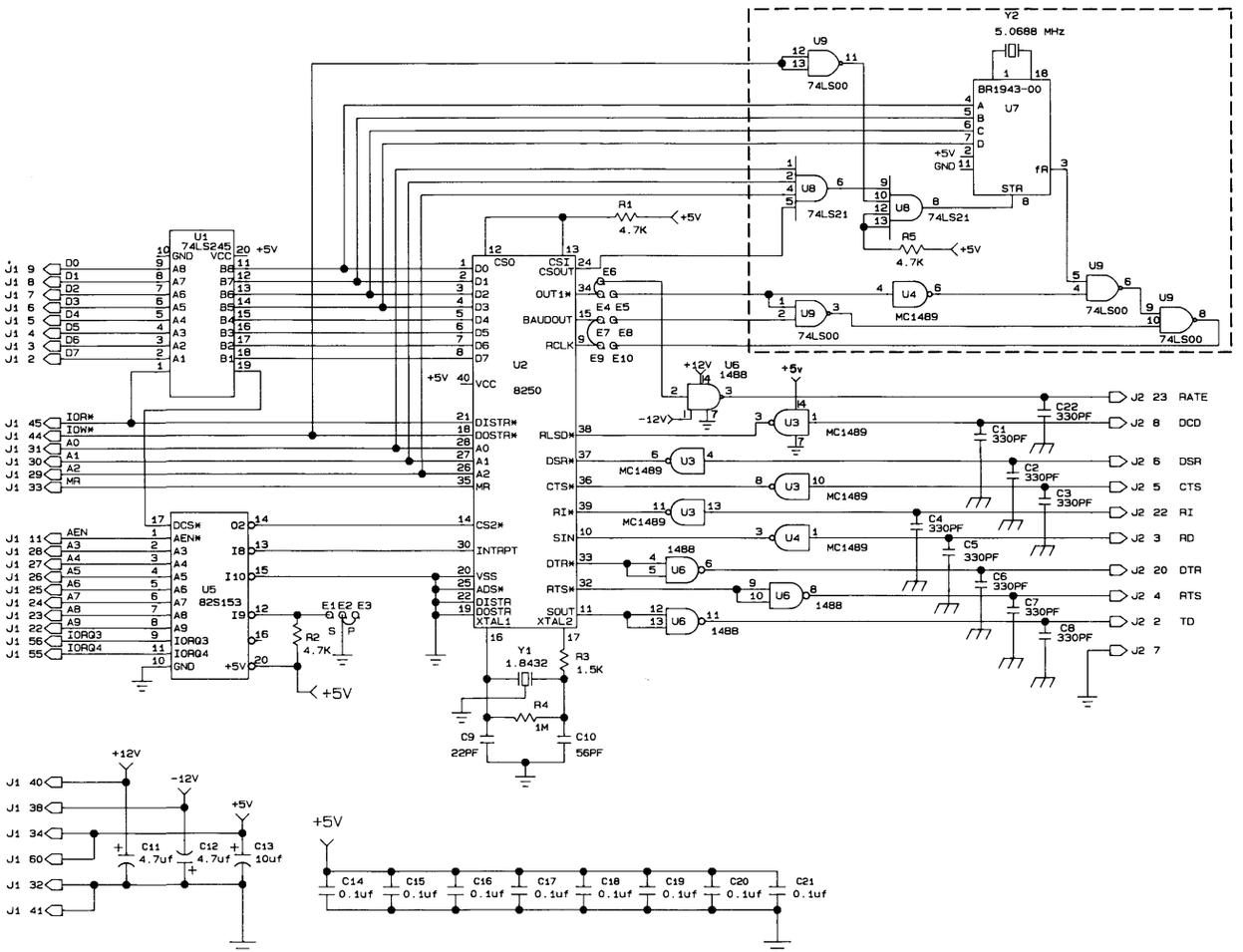
REVISION				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED
	—	RELEASE FOR PRODUCTION	5/22/85	
	A	U3- +5v WAS +12v; ADDED PIN NO'S. PER TCO S12776 kn	5/20/86	



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DRAFT	DATE	TITLE	SCHEMATIC– RS-232 COMBO TANDY 1000
CHECK	DATE		PROJECT NO. 652
DESIGN	DATE		
APPD	DATE		
APPD	DATE		
tandy		DWG NO 8000253	SIZE D
		SCALE —	SHEET 1 OF 1

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8/ WD8250 Asynchronous Communications Element

WESTERN DIGITAL
C O R P O R A T I O N

WD8250 Asynchronous Communications Element

FEATURES

- Designed to be Easily Interfaced to Most Popular Microprocessors (Z-80, 8080A, 6800, etc.)
- Full Double Buffering
- Independently Controlled Transmit, Receive, Line Status, and Data Set Interrupts
- Programmable Baud Rate Generator Allows Division of Any Input Clock by 1 to (2^{16} - 1) and Generates the Internal 16x Clock
- Independent Receiver Clock Input
- Fully Programmable Serial-Interface Characteristics
  - —5-, 6-, 7-, or 8-Bit Characters
  - —Even, Odd, or No-Parity Bit Generation and Detection
  - —1-, 1½-, or 2-Stop Bit Generation
  - —Baud Rate Generation (DC to 56K Baud)
- False Start Bit Detector
- Complete Status Reporting Capabilities
- THREE-STATE TTL Drive Capabilities for Bi-directional Data Bus and Control Bus
- Line Break Generation and Detection
- Internal Diagnostic Capabilities
  - —Loopback Controls for Communications Link Fault Isolation
  - —Break, Parity, Overrun, Framing Error Simulation
- Full Prioritized Interrupt System Controls
- Single +5-Volt Power Supply

GENERAL DESCRIPTION

The WD8250 is a programmable Asynchronous Communication Element (ACE) in a 40-pin package. The device is fabricated in N/MOS silicon gate technology.

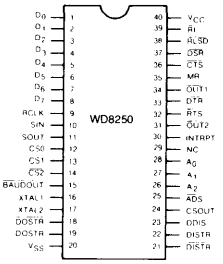
The ACE is a software-oriented device using a three-state 8-bit bi-directional data bus.

The ACE is used to convert parallel data to a serial format on the transmit side, and convert serial data to parallel on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and one half (five bit format only) or two stop bits. The maximum recommended data rate is 56K baud.

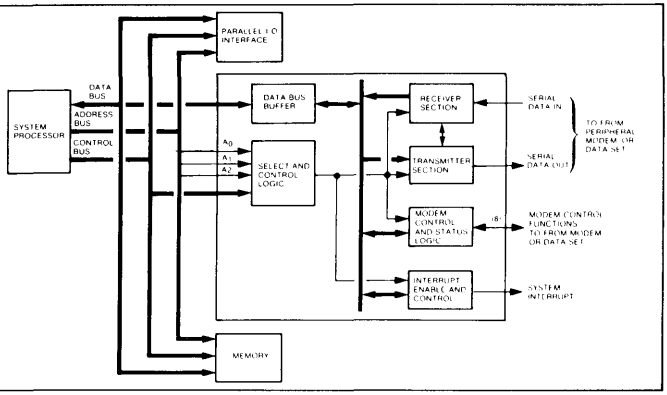
Internal registers enable the user to program various types of interrupts, modem controls, and character formats. The user can read the status of the ACE at any time monitoring word conditions, interrupts and modem status.

An additional feature of the ACE is a programmable baud rate generator that is capable of dividing an internal XTAL or TTL signal clock by a division of 1 to 2^{16} – 1.

The ACE is designed to work in either a polling or interrupt driven system, which is programmable by users software controlling an internal register.



PIN DESIGNATION



WD8250 GENERAL SYSTEM CONFIGURATION

PIN DEFINITIONS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1-8	DATA BUS	D0-D7	3-state input/output lines. Bi-directional communication lines between WD8250 and Data Bus. All assembled data TX and RX, control words, and status information are transferred via the D0-D7 data bus.
9	RECEIVE CLK.	RCLK	This input is the 16X baud rate clock for the receiver section of the chip (may be tied to BAUDOUT pin 15).
10	SERIAL INPUT	SIN	Received Serial Data In from the communications link (Peripheral device, modem or data set).
11	SERIAL OUTPUT	SOUT	Transmitted Serial Data Out to the communication link. The SOUT signal is set to a (logic 1) marking condition upon a MASTER RESET.
12 13 14	CHIP SELECT CHIP SELECT CHIP SELECT	CS0 CS1 $\overline{CS2}$	When CS0 and CS1 are high, and $\overline{CS2}$ is low, chip is selected. Selection is complete when the address strobe $\overline{ADS}$ latches the chip select signals.
15	BAUDOUT	$\overline{BAUDOUT}$	16X clock signal for the transmitter section of the WD8250. The clock rate is equal to the oscillator frequency divided by the divisor loaded into the divisor latches. The BAUDOUT signal may be used to clock the receiver by tying to (pin 9) RCLK.
16 17	EXTERNAL CLOCK IN EXTERNAL CLOCK OUT	XTAL 1 XTAL 2	These pins connect the crystal or signal clock to the WD8250 baud rate divisor circuit. See Fig. 3 and Fig. 4 for circuit connection diagrams.
18 19	DATA OUT STROBE DATA OUT STROBE	$\overline{DOSTR}$ DOSTR	When the chip has been selected, a low $\overline{DOSTR}$ or high DOSTR will latch data into the selected WD8250 register (a CPU write). Only one of these lines need be used. Tie unused line to its inactive state. $\overline{DOSTR}$ — high or DOSTR — low.
20	GROUND	V_{SS}	System signal ground.
21 22	DATA IN STROBE DATA IN STROBE	$\overline{DISTR}$ DISTR	When chip has been selected, a low $\overline{DISTR}$ or high DISTR will allow a read of the selected WD8250 register (a CPU read). Only one of these lines need be used. Tie unused line to its inactive state. $\overline{DISTR}$ — high or DISTR — low.
23	DRIVER DISABLE	DDIS	Output goes low whenever data is being read from the WD8250. Can be used to reverse data direction of external transceiver.
24	CHIP SELECT OUT	CSOUT	Output goes high when chip is selected. No data transfer can be initiated until CSOUT is high.
25	ADDRESS STROBE	$\overline{ADS}$	When low, provides latching for register. Select (A0, A1, A2) and chip select (CS0, CS1, $\overline{CS2}$) NOTE: An active $\overline{ADS}$ signal is required when the Register Select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required, the $\overline{ADS}$ input can be tied permanently low.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
26 27 28	REGISTER SELECT A2 REGISTER SELECT A1 REGISTER SELECT A0	A2 A1 A0	These three inputs are used to select a WD8250 internal register during a data read or write. See Table below.
29	NO CONNECT	NC	No Connect
30	INTERRUPT	INTRPT	Output goes high whenever an enabled interrupt is pending.
31	OUTPUT 2	$\overline{OUT2}$	User-designated output that can be programmed by Bit 3 of the modem control register = 1, causes $\overline{OUT2}$ to go low.
32	REQUEST TO SEND	$\overline{RTS}$	Output when low informs the modem or data set that the WD8250 is ready to transmit data. See Modem Control Register.
33	DATA TERMINAL READY	$\overline{DTR}$	Output when low informs the modem or data set that the WD8250 is ready to communicate.
34	OUTPUT 1	$\overline{OUT1}$	User designated output can be programmed by Bit 2 of Modem Control Register = 1 causes $\overline{OUT1}$ to go low.
35	MASTER RESET	MR	When high clears the registers to states as indicated in Table 1.
36	CLEAR TO SEND	$\overline{CTS}$	Input from DCE indicating remote device is ready to transmit. See Modem Control Register.
37	DATA SET READY	$\overline{DSR}$	Input from DCE used to indicate the status of the local data set. See Modem Control Register.
38	RECEIVED LINE SIGNAL DETECT	$\overline{RSLD}$	Input from DCE indicating that it is receiving a signal which meets its signal quality conditions. See Modem Control Register.
39	RING INDICATOR	$\overline{RI}$	Input, when low, indicates that a ringing signal is being received by the modem or data set. See Modem Control Register.
40	+5V	V_{CC}	+5 Volt Supply.

CHIP SELECTION AND REGISTER ADDRESSING

Address Strobe (ADS pin 25): When low provides latching for register select (A0, A1, A2) and chip select (CS0, CS1, $\overline{CS2}$).

NOTE: An active $\overline{ADS}$ input is required when register select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If $\overline{ADS}$ is not required for latching, tie this input permanently low.

Chip Select (CS0, CS1, $\overline{CS2}$) pins 12-14: The definition of chip selected is CS0, CS1 both high and $\overline{CS2}$ is low. Chip selection is complete when latched by $\overline{ADS}$ or $\overline{ADS}$ is tied low.

Register Select (A0, A1, A2) pins 26-28: To select a register for read or write operation, see Register Table.

NOTE: (DLAB) Divisor Latch access bit is the MSB of the Line Control Register. DLAB must be programmed high logic 1 by the system software to access the Baud Rate Generator Divisor Latches.

DLAB	A2	A1	A0	Register
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	None
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

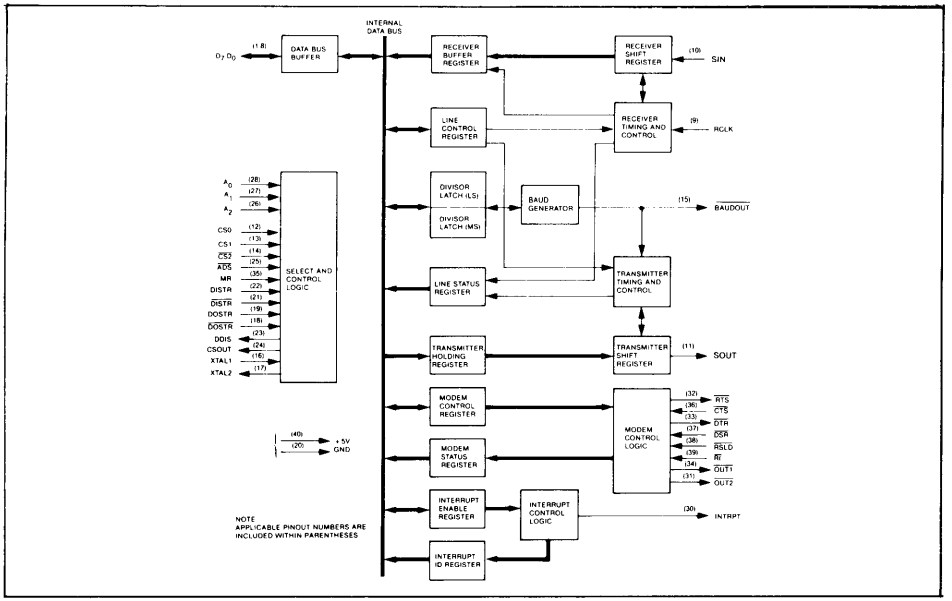
WD8250 OPERATIONAL DESCRIPTION

Master Reset

A high-level input on pin 35 causes the WD8250 to reset to the condition listed in Table 1.

WD8250 Accessible Registers

The system programmer has access to any of the registers summarized in Table 2. For individual register descriptions, refer to the following pages under register heading.



WD8250 BLOCK DIAGRAM

Table 1. Reset Control of Registers and Pinout Signals

Register/Signal	Reset Control	Reset State
Receiver Buffer Register	First Word Received	Data
Transmitter Holding Register	Writing into the Transmitter Holding Register	Data
Interrupt Enable Register	Master Reset	All Bits Low (0-3 forced and 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High and Bits 1-7 Are Permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, Except Bits 5 and 6 Are High
Modem Status Register	Master Reset MODEM Signal Inputs	Bits 0-3 Low Bits 4-7 — Input Signal
Divisor Latch (low order bits)	Writing into the Latch	Data
Divisor Latch (high order bits)	Writing into the Latch	Data
SOUT	Master Reset	High
$\overline{\text{BAUDOUT}}$	Writing into either Divisor Latch	Low
CSOUT	$\overline{\text{ADS}}$ Strobe Signal and State of Chip Select Lines	High/Low
DDIS	DDIS = $\overline{\text{CSOUT}} \cdot \text{RCLK} \cdot \overline{\text{DISTR}}$ (At Master Reset, the CPU sets RCLK and DISTR low.)	High
INTRPT	Master Reset	Low

$\overline{OUT\ 2}$	Master Reset	High
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
$\overline{OUT\ 1}$	Master Reset	High
D7-D0 Data Bus Lines	In THREE-STATE Mode, Unless CSOUT • DISTR = High or CSOUT • DOSTR = High	THREE-STATE Data (ACE to CPU) Data (CPU to ACE)

Table 2. Summary of WD8250 Accessible Registers

	Register Address									
	0 DLAB=0	0 DLAB=0	1DLAB=0	2	3	4	5	6	0DLAB=1	1DLAB=1
Bit No.	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Identification Register	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Divisor Latch (LS)	Divisor Latch (MS)
0	Data Bit 0*	**Data Bit 0***	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	Word Length Select Bit 1 WLS1)	Request to Send (RTS)	Overrun Error (OR)	Delta Data Set Ready (DDSR)	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	0	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Receive Line Signal Detect (DSLSD)	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register Empty (THRE)	Data Set Ready (DSR)	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Shift Register Empty (TSRE)	Ring Indicator (RI)	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Received Line Signal Detect (RLSD)	Bit 7	Bit 15

*Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Line Control Register

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of stop bits in each transmitted or received serial character. If bit 2 is a logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, 1½ Stop bits are generated or checked. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, 2 Stop bits are generated or checked.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the Parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state and remains there (until reset by a low-level bit 6) regardless of other transmitter activity. The feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

WD8250 Programmable Baud Rate Generator

The WD8250 contains a programmable Baud Rate Generator that is capable of taking any clock input (DC to 3.1 MHz) and dividing it by any divisor from 1 to (2^{16} - 1). The output frequency of the Baud Generator is 16x the Baud rate. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 3 and 4 illustrate the use of the Baud Generator with two different driving frequencies. One is referenced to a 1.8432 MHz crystal. The other is a 3.072 MHz crystal.

NOTE

The maximum operating frequency of the Baud Generator is 3.1 MHz. However, when using divisors of 6 and below, the maximum frequency is equal to 1/2 the divisor in MHz. For example, if the divisor is 1, then the maximum frequency is 1/2 MHz. In no case should the data rate be greater than 56K Baud.

Line Status Register

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of

Table 3. Baud Rates Using 1.8432 MHz Crystal.

Desired Baud Rate	Divisor Used to Generate 16x Clock	Percent Error Difference Between Desired and Actual
50	2304	—
75	1536	—
110	1047	0.026
134.5	857	0.058
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.69
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	2.86

NOTE: 1.8432 MHz is the standard 8080 frequency divided by 10.

Table 4. Baud Rates Using 3.072 MHz Crystal.

Desired Baud Rate	Divisor Used to Generate 16x Clock	Percent Error Difference Between Desired and Actual
50	3840	—
75	2560	—
110	1745	0.026
134.5	1428	0.034
150	1280	—
300	640	—
600	320	—
1200	160	—
1800	107	—
2000	96	—
2400	80	—
3600	53	0.628
4800	40	—
7200	27	1.23
9600	20	—
19200	10	—
38400	5	—
56000	3	14.285

the Line Status Register are indicated in table 2 and are described below.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 may be reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register or by writing a logic 0 into it from the CPU.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level).

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (Logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits).

NOTE

Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the WD8250 is ready to accept a new character for transmission. In addition, this bit causes the WD8250 to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Shift Register Empty (TSRE) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Shift Register is idle. It is reset to logic 0 upon a data transfer from the Transmitter Holding Register to the Transmitter Shift Register. Bit 6 is a read-only bit.

Bit 7: This bit is permanently set to logic 0.

Interrupt Identification Register

The WD8250 has an on chip interrupt capability that allows for complete flexibility in interfacing to all popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the WD8250 prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and source of that interrupt are stored in the Interrupt Identification Register (refer to table 5). The Interrupt Identification Register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in table 2 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in table 5.

Bits 3 through 7: These five bits of the IIR are always logic 0.

Interrupt Enable Register

This 8-bit register enables the four interrupt sources of the WD8250 to separately activate the chip Interrupt (INTRPT) output signal. It is possible to totally disable the interurpt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are indicated in table 2 and are described below.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1. Bit 0 is reset to logic 0 upon completion of a read of the Receiver Buffer Register.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to a logic 1. Bit 1 is reset to logic 0 upon a write to the Transmitter Holding Register.

Table 5. Interrupt Control Functions.

Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1. Bit 2 is reset to logic 0 upon completion of the associated interrupt service routine.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1. Bit 3 is reset to logic 0 upon completion of the associated interrupt service routine.

Bits 4 through 7: These four bits are always logic 0.

MODEM Control Register

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in table 2 and are described below.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

NOTE

The $\overline{DTR}$ output of the WD8250 may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 ($\overline{OUT\ 1}$) signal, which is an auxiliary user-designated output. Bit 2 affects the $\overline{OUT\ 1}$ output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output 2 ($\overline{OUT\ 2}$) signal, which is an auxiliary user-designated output. Bit 3 affects the $\overline{OUT\ 2}$ output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a loopback feature for diagnostic testing of the WD8250. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the HIGH IMPEDANCE state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$, and $\overline{RI}$) are disconnected; and the four MODEM Control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT\ 1}$, and $\overline{OUT\ 2}$) are internally connected to the four MODEM Control inputs. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit- and receive-data paths of the WD8250.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

The WD8250 interrupt system can be tested by writing into the lower six bits of the Line Status Register

and the lower four bits of the MODEM Status Register. Setting any of these bits to a logic 1 generates the appropriate interrupt (if enabled). The resetting of these interrupts is the same as in normal WD8250 operation. To return to this operation, the registers must be reprogrammed for normal operation and then bit 4 must be reset to logic 0.

Bits 5 through 7: These bits are permanently set to logic 0.

MODEM Status Register

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in table 2 and are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from an On (logic 1) to an Off (logic 0) condition.

Bit 3: This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 indicates that the $\overline{RLSD}$ input to the chip has changed state.

NOTE

Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{DSR}$) input.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input.

Bit 7: This bit is the complement of the Received Line Signal Detect ($\overline{RLSD}$) input.

Typical Applications

Figures 1 and 2 show how to use the WD8250 chip in an 8080A system and in a microcomputer system with a high-capacity data bus.

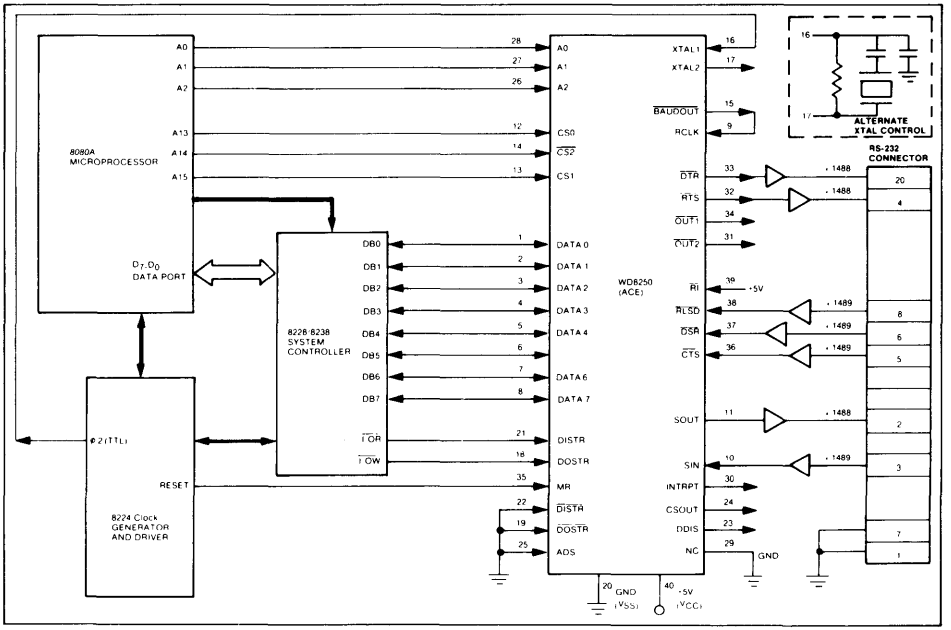


FIGURE 1. TYPICAL 8-BIT MICROPROCESSOR/RS-232 TERMINAL INTERFACE USING THE ACE.

Typical Applications (continued)

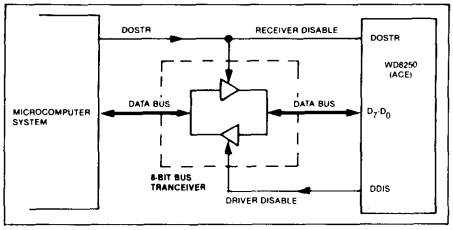


FIGURE 2. TYPICAL INTERFACE FOR A HIGH-CAPACITY DATA BUS.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... 0°C to +70°C
Storage Temperature -65°C to +150°C (Ceramic)
-50°C to +125°C (Plastic)
All Input or Output Voltages with
Respect to V_{SS} ..... -0.5 V to +7.0 V
Power Dissipation ..... 750 mW

Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.

DC Electrical Characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ± 5%, V_{SS} = 0V, unless otherwise specified.

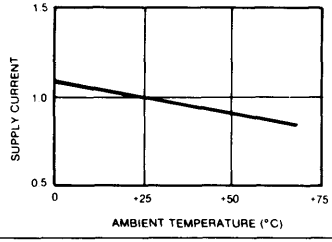
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V_{ILX}	Clock Input Low Voltage	-0.5		0.8	V	
V_{IHX}	Clock Input High Voltage	2.0		VCC	V	
V_{IL}	Input Low Voltage	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.4		VCC	V	
V_{OL}	Output Low Voltage			.45	V	I_{OL}=1.6mA on all outputs
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-100 μA
$I_{CC(AV)}$	Avg Power Supply Current (V_{CC})			150	ma	
I_{IL}	Input Leakage			± 10	μA	
I_{CL}	Clock Leakage			± 10	μA	
I_{DL}	Data Bus Leakage			± 10	μA	V_{OUT} = 0.4V, V_{OUT} = 4.6V: Data Bus is at High-Impedance State

Capacitance

T_A = 25°C, V_{CC} = V_{SS} = 0V

Symbol	Parameter	Typ.	Max.	Units	Test Conditions
C_{XIN}	Clock Capacitance	10	15	pF	fc=1 MHz, Unmeasured pins returned to V_{SS}
C_{IN}	Input Capacitance	6	10	pF	
C_{OUT}	Output Capacitance	10	20	pF	

Typical Supply Current vs. Temperature, Normalized

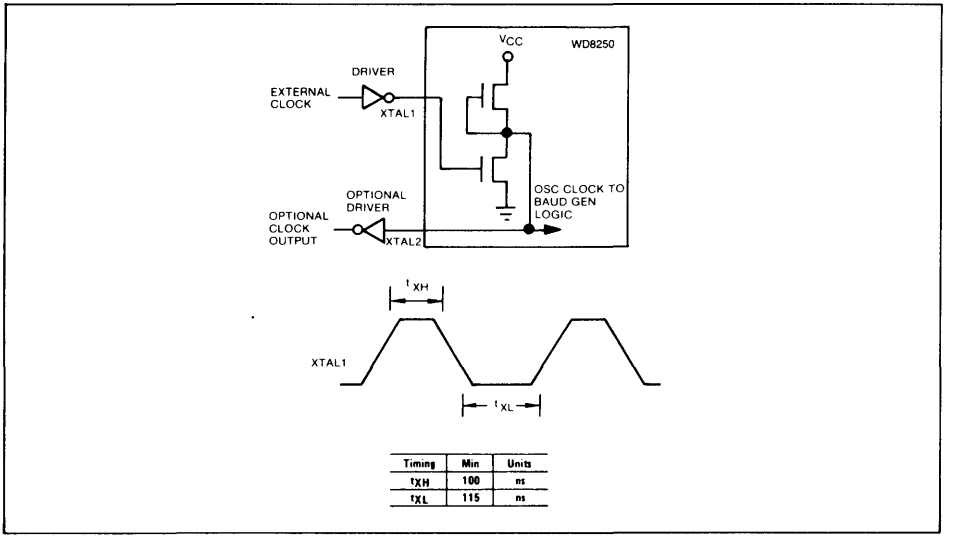


AC Electrical Characteristic TA = 0°C to +70°C, V_{CC} = +5V ± 5%

Symbol	Parameter	Units	Min	Max	Test Conditions
t_{AW}	Address Strobe Width	ns	120		1TTL Load
t_{ACS}	Address and Chip Select Setup Time	ns	100		1TTL Load
t_{AH}	Address Hold Time	ns	0		1TTL Load
t_{CSS}	Chip Select Output Delay from Latch	ns		160	1TTL Load
t_{DID}	$\overline{DISTR}$/DISTR Delay from Latch	ns	50		1TTL Load
t_{DIW}	$\overline{DISTR}$/DISTR Strobe Width	ns	300		1TTL Load
t_{RC}	Read Cycle Delay	ns	655		1TTL Load
RC	Read Cycle = t_{ACS} + t_{DID} + t_{DIW} + t_{RC} + 20 ns	ns	1125		1TTL Load
t_{DD}	$\overline{DISTR}$/DISTR to Driver Disable Delay	ns		200	1TTL Load
t_{DDD}	Delay from $\overline{DISTR}$/DISTR to Data	ns		300	1TTL Load
t_{HZ}	$\overline{DISTR}$/DISTR to Floating Data Delay	ns	60		1TTL Load
t_{DOD}	$\overline{DOSTR}$/DOSTR Delay From Latch	ns	20		1TTL Load
t_{DOW}	$\overline{DOSTR}$/DOSTR Strobe Width	ns	175		1TTL Load
t_{WC}	Write Cycle Delay	ns	685		1TTL Load
WC	Write Cycle = t_{ACS} + t_{DOD} + t_{DOW} + t_{WC} + 20 ns	ns	1000		1TTL Load
t_{DS}	Data Setup Time	ns	175		1TTL Load
t_{DH}	Data Hold Time	ns	60		1TTL Load
t_{CSC}	Chip Select Output Delay from Select	ns		260	1TTL Load
t_{DIC}	$\overline{DISTR}$/DISTR Delay from Select	ns	150		1TTL Load
t_{DOC}	$\overline{DOSTR}$/DOSTR Delay from Select	ns	150		1TTL Load

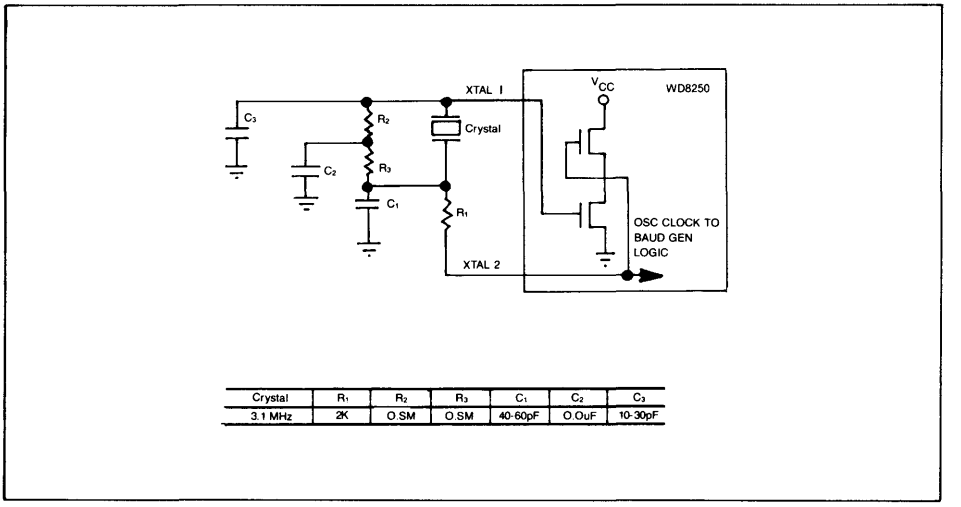
Symbol	Parameter	Min.	Max.	Units	Test Conditions
Baud Generator					
N	Baud Rate Divisor	1	$2^{16}-1$		
t_{BLD}	Baud Output Negative Edge Delay		250 typ	ns	100pF Load
t_{BHD}	Baud Output Positive Edge Delay		250 typ	ns	100pF Load
t_{LW}	Baud Output Down Time	425 Typ		ns	100pF Load
t_{HW}	Baud Output Up Time	330 Typ		ns	100pF Load
Receiver					
t_{SCD}	Delay from RCLK to Sample Time		2 typ	μs	
t_{SINT}	Delay from Stop to Set Interrupt		2 typ	μs	100pF Load
t_{RINT}	Delay from $\overline{DISTR}$/DISTR (RD RBR) to Reset Interrupt	.250	1 typ	μs	100pF Load
Transmitter					
t_{HR}	Delay from $\overline{DOSTR}$/DOSTR (WR THR) to Reset Interrupt	.250	1 typ	μs	100pF Load
t_{IRS}	Delay from Initial INTR Reset to Transmit Start		16 typ	$\overline{BAUDOUT}$ Cycles	
t_{SI}	Delay from Initial Write to Interrupt		24 typ	$\overline{BAUDOUT}$ Cycles	
t_{SS}	Delay from Stop to Next Start	.250	1 typ	μs	
t_{STI}	Delay from Stop to Interrupt (THRE)		8 typ	$\overline{BAUDOUT}$ Cycles	
TIR	Delay from $\overline{DISTR}$/DISTR (RD IIR) to Reset Interrupt (THRE)	.250	1 typ	μs	100pF Load
Modem Control					
t_{MDO}	Delay from DOSTR/$\overline{DOSTR}$ (WR MCR) to Output	.250	1 typ	μs	100pF Load

t_{SIM}	Delay to Set Interrupt from MODEM Input	.250	1 typ	μs	100pF Load
t_{RIM}	Delay to Reset Interrupt from $\overline{DISTR}$/DISTR (RD MSR)	.250	1 typ	μs	100pF Load



Timing	Min	Units
t_{XH}	100	ns
t_{XL}	115	ns

FIGURE 3. EXTERNAL CLOCK INPUT (3.1 MHz MAX.)



Crystal	R_1	R_2	R_3	C_1	C_2	C_3
3.1 MHz	2K	O.SM	O.SM	40-60pF	O.OuF	10-30pF

FIGURE 4. TYPICAL CRYSTAL OSCILLATOR NETWORK

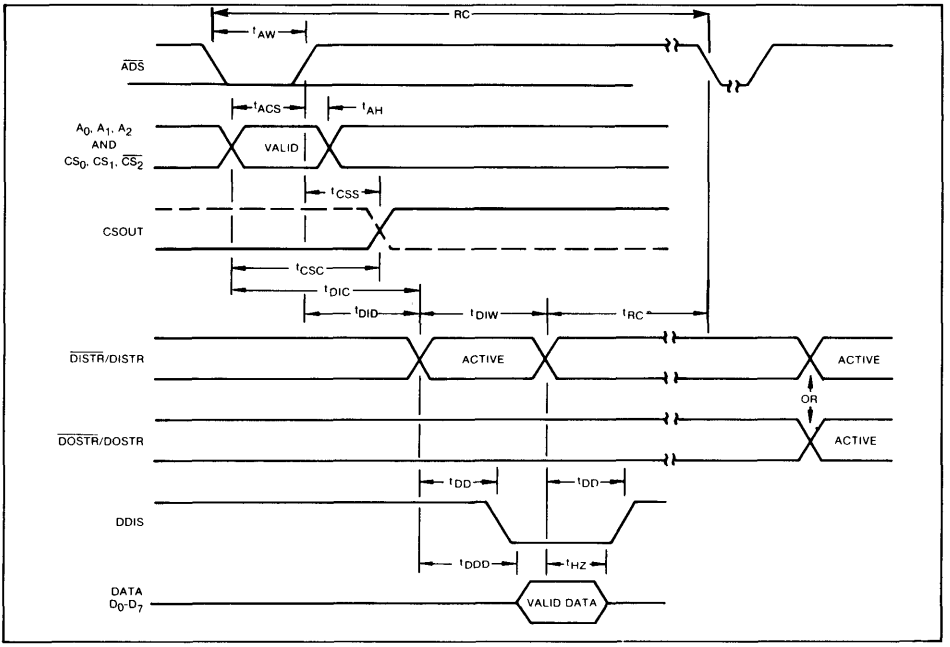


FIGURE 5. READ CYCLE TIMING

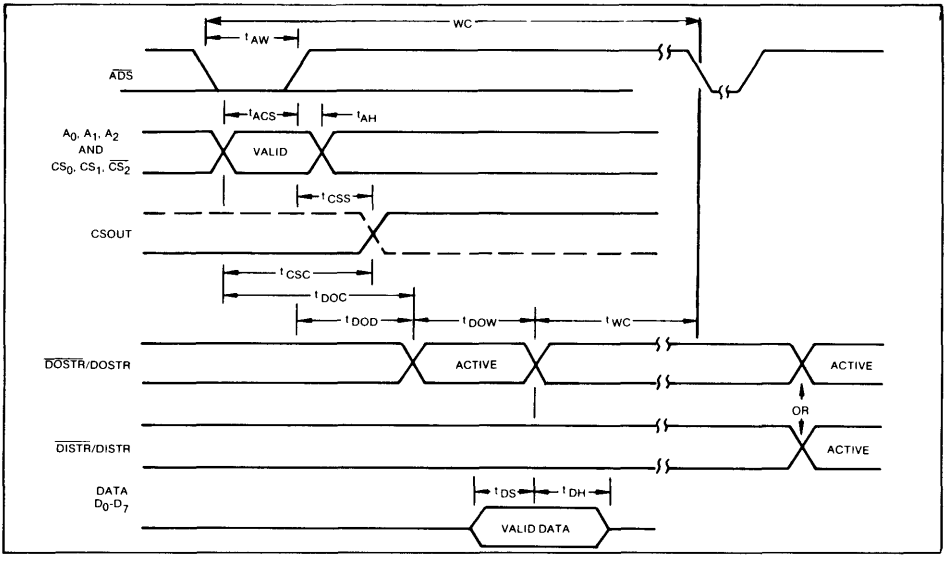


FIGURE 6. WRITE CYCLE TIMING

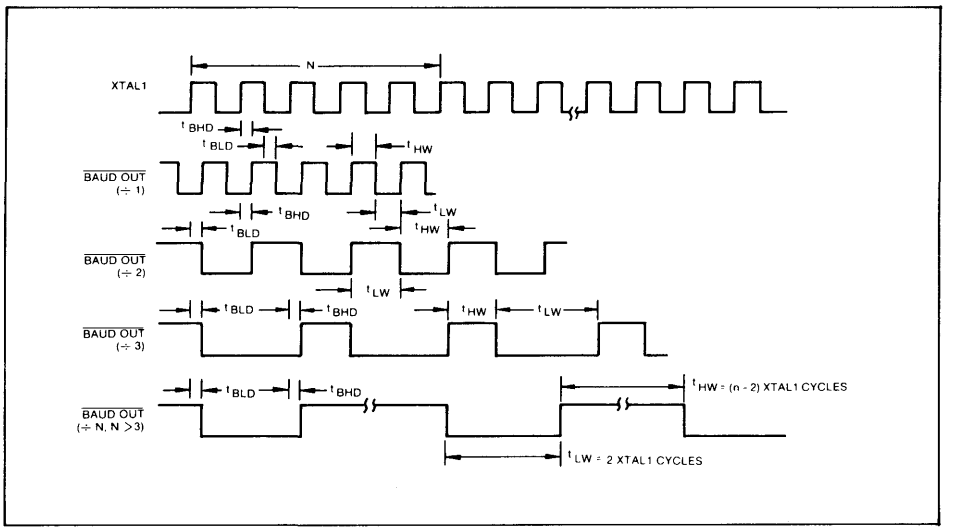
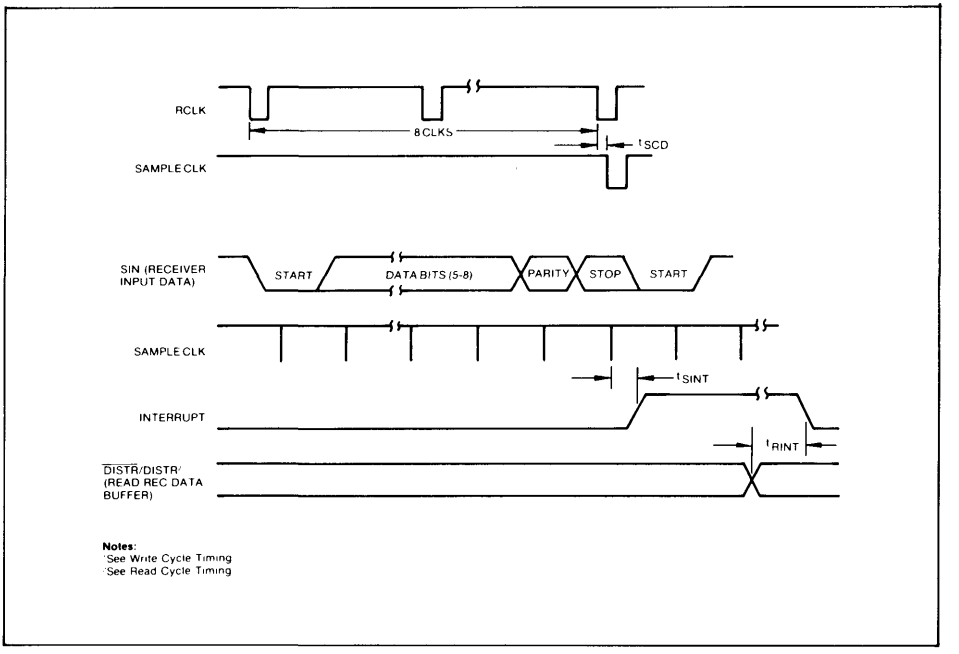
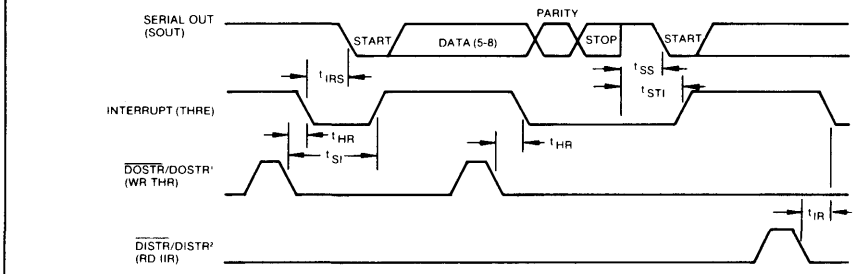


FIGURE 7. BAUDOUT TIMING



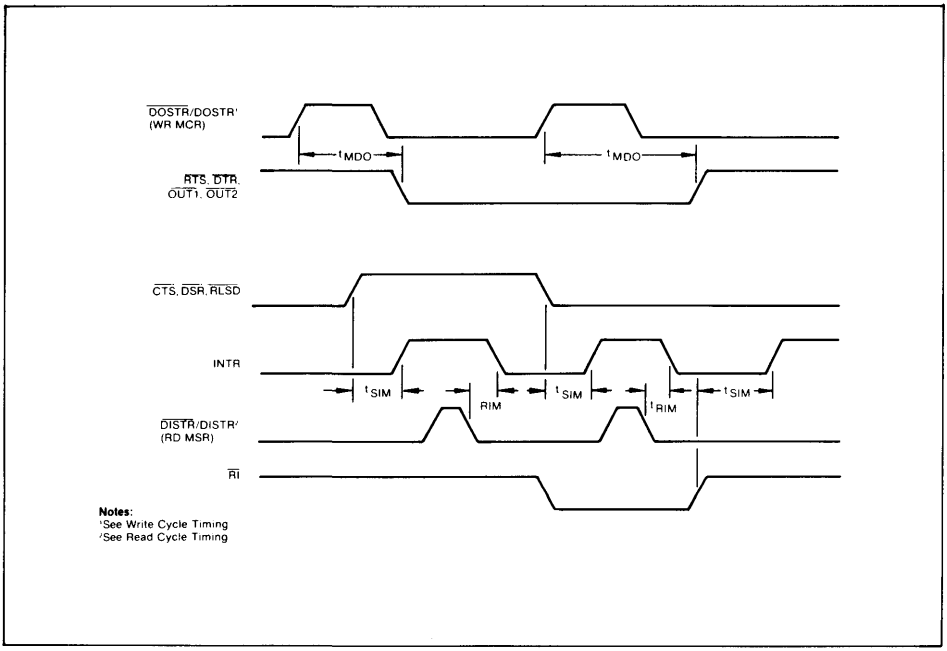
Notes:
[1]See Write Cycle Timing
[2]See Read Cycle Timing

FIGURE 8. RECEIVER TIMING



Notes:
[1]See Write Cycle Timing
[2]See Read Cycle Timing

FIGURE 9. TRANSMITTER TIMING



Notes:
[1]See Write Cycle Timing
[2]See Read Cycle Timing

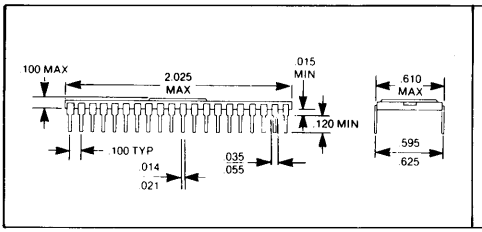
FIGURE 10. MODEM CONTROLS TIMING

ORDERING INFORMATION

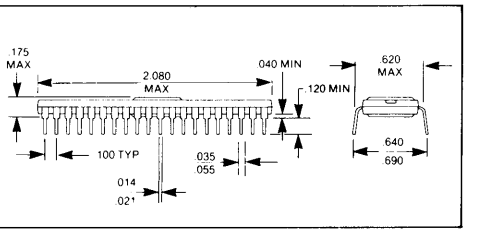
Part Number	Max Clock Rate[1]	Bits/Character
WD8250*-00	3.1 MHz	5, 6, 7, 8
WD8250*-20	3.1 MHz	6, 7, 8
WD8250*-30	500 kHz	5, 6, 7, 8

NOTES:

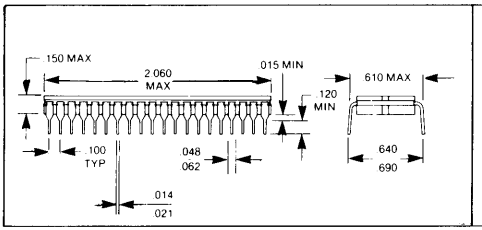
1. This is the maximum clock rate that can be applied to pins 16 or 17.
   * Consult your local Western Digital Sales Representative for information regarding package availability, price, and delivery.



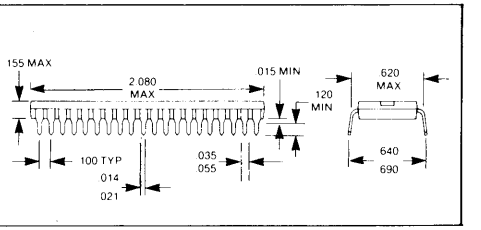
40 LEAD CERAMIC "A" or "AL"



40 LEAD RELPACK "B" or "BL"



40 LEAD CERDIP "CL"



40 LEAD PLASTIC "P" or "PL"

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Tandy® 1000 Mouse Controller/Calendar

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1/ Introduction

The Mouse Controller/Calender Board interfaces the DIGI-Mouse pointing device (Cat. No. 26-1197) to the Tandy 1000. The application programs that require the DIGI-Mouse pointing device can be used on the Tandy 1000. Also the battery backed clock/calendar allows the user to run the software provided on the diskette that comes with the owner's manual.

2/ Specifications

Dimensions: Standard half size board (5 x 8.2 inches).

Battery: 3.0-Volt Lithium coin cell, type CR2320 (Cat. No. 23-163). The battery life is one year.

Processor: 8042 8-bit single chip processor.

Clock Speed: 7.16 MHz

Ambient Temperature Range:
55° to 95° F (12° to 35° C)

Storage Temperature Range:
-40° to +160° F (-40° to 71° C)

3/ Theory of Operation (Hardware)

Look at the block diagram (Figure 1) and the clock/calendar schematic while reading the information below.

Bus I/F

Data, address, and control signals of the 1000 interface bus are buffered by U9 (an octal bus transceiver) and U7 (an octal buffer/line driver with 3-state outputs).

Chip Select and Reset Logic

The address lines are decoded by U2, U5, and U6. When the 1000 writes or reads to Ports 2FC or 2FE, a chip select signal is generated at Pin 6 of U2. The chip select controls U9 (the data buffer) and U3 (the 8042 processor).

During DMA cycles, the AEN signal from the 1000 bus, disables the chip select signal at Pin 1 of U7. An active AEN signal disables the 1Y outputs of U7, causing the A08 signal from Pin 12 of U7 to float and be pulled high by R20. U5 then inverts the A08 signal, ensuring that the chip select is disabled during DMA.

One half of U1 (a dual D-type flip-flop) is used in a "divide by 2" configuration. The 14.32 MHz oscillator signal from the 1000 interface bus is divided in half for a clock speed of 7.14 MHz, to be used by the 8042 processor. The 7.14 MHz clock is at Pin 5 of U1.

The other half of U1 is used as a reset latch. A reset signal is provided for the 8042 processor by ORing together the System Reset signal from the computer interface bus and the signal from the reset latch at Pin 11 of U2. The 8042 processor can be reset by a system reset or a write to I/O port 2FF. A write to I/O port 2FD clears the reset signal.

8042 Processor

In the heart of the option board is the 8042 processor (U3). This processor acts as an input port for serial information from the DIGI-Mouse and the Clock/Calendar chip (U8). It then translates this information to a parallel format and controls its transfer to the computer interface bus. The Clock/Calendar option board uses interrupt request IRQ3 to inform the 1000 when it is ready to transfer data.

DIGI-Mouse Buffers and Filters

A 9-Pin DB jack at J2 connects the DIGI-Mouse to the clock/ calendar board. RC filtering is used to reduce noise in the inputs. U4 (a CMOS hex schmitt trigger) provides further buffering and waveshaping of the DIGI-Mouse inputs, which are interfaced to the processor chip through its peripheral port bits P10 to P16.

Clock Chip

The Phillips-Signetics Clock/Calendar Chip (U8) interfaces directly to U3 at its peripheral port bits P17, P20-P23, and P27. The time base for the clock chip is a 32.768 KHz crystal, which is similar to that found in watches. The battery **MUST** be installed for the clock function to work. When a power failure occurs, the chip indicates this by sending a low-battery signal (POWF) to the 8042 processor.

4/ Theory of Operation (Software)

User specifications:

- The motion sensor is oriented with the connecting cable and buttons pointing away from the user, the positive x axis extends to the right and the positive y axis extends toward the user.
- Minimum motion allowed before it is detected is 1/79 of an inch along either axis. This distance is called a tick.
- The minimum unit of time for the Clock/Calendar chip is 1 minute. Maximum accuracy is ± 1/2 minute. The units of time accepted by the chip are minutes, (24) hours, day of month, and month.
- There are 3 modes for the mouse's motion data and button data that can be transfered to the host: the full interrupt mode, the initial interrupt and poll mode, and the poll only mode.
- To communicate with the clock/calendar chip, the user employs the set time command and a read time command.

I/O Ports used by the Clock/Calendar Board:

8042 Data Port	2FC
8042 Command/Status Port	2FE
8042 Set RESET 8042 Port	2FF
8042 Clear RESET 8042 Port	2FD

Layout of the 8042's status port (2FE):

Read by the 8088:

Bit #0 = Output register full flag (OBF)	1=full
Bit #1 = Input register full flag (IBF)	1=full
Bit #2 = F0 flag - not used	
Bit #3 = F1 flag - command flag	1=input to port 2FE
Bit #4 = Primary button status	1=button up
Bit #5 = Secondary button status	1=button up
Bit #6 = Tertiary button status	1=button up
Bit #7 = Calendar power status	1=power has failed

Written to by the 8088:

This is the same as for the data written to Data Port 2FC, except the F1 (command) flag in 8042's status port is set.

Output:

When sending data or commands from the 8088 to the 8042, the following procedure must be used:

1. Check the status port (2FE) of the 8042 to see if the input port full flag is set (Bit 1).

2. If the flag is set, wait until the 8042 clears it. If it is not cleared within 1 millisecond, reset the 8042 chip because it is locked up.

3. If the flag is clear, proceed.

4. Check the length of the command. If it is equal to 1, then send the data to 2FE, and stop here.

5. If the length equals 2 or more, then send the data to 2FC, and proceed.

6. Wait until the input port full flag is cleared by the 8042 before sending the next byte of data to 2FC.

7. When the length equals 1, send it to 2FE, and stop here.

Formats of Commands to the 8042:

Command	Header	Data
Set Time	01h	All data must be in BCD format. 1st byte = minutes. 2nd byte = hours (24 hour clock). 3rd byte = day of the month. 4th byte = month.
Read Time	02h	None Returns data packet "R".
Set Mouse Motion Interrupt and	08h	Output is 2 bytes. 0 = disable function. 1 - 255 = net number of "ticks" to be moved before interrupt is triggered. Returns data packet "M".

Button Interrupt		0 = disable function. 1 - 255 = enable function Returns data packet "B".
Set Timer Interrupt	20h	Outputs 1 byte of data 0 = disable function. 1 - 255 = enable function Returns data packet "A".

(Timer is set to interrupt approximately 40 times per second if the data is available to send.)

What is happening:

The 8042 is interrupted every time data is written to the input port 2FC (or 2FE, which set the command flag). The 8042 moves the data from the input register into the input buffer and increments a counter. It then returns to the point in the mouse data sampling and processing cycle at the point of interruption.

During each cycle, the 8042 checks the command flag to see if a command has been received. If the command flag is set, the 8042 checks the header byte to determine which command is in its input buffer. It then compares the counter to the number of bytes in that command. If any of these tests fails, the 8042 resets the pointer to the input buffer, clears the counter and the command flag, and continues with its normal cycle. If all the tests succeed, the 8042 jumps to the routine that handles that command. Each command has the requirement to reset the buffer pointer, the counter, and the command flag, and then return control to the normal process.

Input:

Data transfer between the 8042 and the main processor (8088) uses the interrupt mode, the poll mode, or both. The 8042 interrupts the 8088 by toggling Port 21h, Bit 3, which is connected through a buffer to the 8259A interrupt controller chip. The clock/calendar board uses IRQ3 as an interrupt. Internally, the 8042 knows if the 8088 has read/written a byte from/to it by checking the status of the OBF/IBF flags. Three procedures are available to transfer the data from the 8042 to the 8088. They are discussed below.

Mode 1: Full interrupt mode

This mode uses the interrupt line to signal each byte to be transmitted. As each byte is transmitted, the common procedure below is executed except Mode 3 must have the latched interrupt cleared after each byte is processed. This mode may be the fastest mode when only the clock interrupt is actively being triggered.

Mode 2: Initial interrupt and poll mode

This mode uses the interrupt line to signal the start of a data packet, and polls the rest of the packet. It clears the latched interrupt only after all the data packet is transmitted. It uses the common procedure outlined below.

Mode 3: Poll only mode

This mode does not use the interrupt signal at all. It uses only the output register full flag in the 8042's status register (Port 2FE).

Common procedure:

The 8088 must have the following initialized before any interrupt mode is used:

- A hardware interrupt vector at 002C.
- An interrupt controller at port 21 (ANDed with a F7).

The 8042 has a data packet set up in its output buffer and begins transmitting by placing the "header" into the output register (Port 2FC). Placing the header byte into the ouput register sets the output register full flag in the status register (Port 2FE, Bit 0) and sends a signal on the interrupt line to the 8088 (via the 8259A). The 8042 begins its normal processing cycle, testing the output register full flag on each cycle.

If the flag is set, the 8042 sends another signal on the interrupt line. If the flag is cleared and the packet still contains data to send, the 8042 places the next data byte into the output register and sends a signal on the interrupt line to the 8088. If the flag is cleared and the data packet is empty, the 8042 does NOT send an interrupt signal, but continues with its normal processing.

On the 8088 side, the "mouse" interrupt has a priority behind the 8253 timer, keyboard, and hard disk. This means that when the interrupt enters its routine, the higher-level interrupts can be enabled. The interrupt handler routine should do all the following:

- Ensure that the 8042 generated the interrupt by checking the status of its output register full flag.
- Identify the type of data packet by its "header" byte and switch to the appropriate routine when the entire data packet is received.
- After the data packet has been processed, clear or reset the buffer pointers, counters, and the latched interrupt.

Format of Data Packets from the 8042:

Data Packet	Header	Data
Mouse data		4 bytes of data
All data	"A"	1st byte = MSB of Delta x
Motion data only	"M"	2nd byte = LSB of Delta x
		3rd byte = MSB of Delta y
		4th byte = LSB of Delta y

(The button data is found in the status register (Port 2FE.)

Mouse data		none
Button data only	"B"	data found in status register (Port 2FE bits # 4, 5, 6)
Read time data	"R"	4 bytes of data in BCD format 1st byte = minutes 2nd byte = hours (24-hour clock) 3rd byte = day of month 4th byte = month

Initialization Procedures of 8088:

The following hardware and software interrupts should be initialized:

Description	Address	Type
Hardware interrupt vector (INT 0B)	002C	Doubleword Pointer
Application interrupt vector (INT 33)	00CC	Doubleword Pointer
Hardware interrupt controller (IRQ3)	Port 21	(reset Bit 3)
Video display interrupt (INT 10)	0040	Doubleword Pointer

Operation of the Clock/Calendar:

When the 8042 receives either the Set Time or Read Time command, it shuts off all other operations until it is finished with the command. All the resources of the 8042 are required to communicate with the clock/calendar chip.

In the Set Time command, the 8042 breaks up the 4 bytes of time data into 4 packets and sends them serially a bit at a time. Upon completion, the 8042 resumes normal operation.

In the Read Time command, the 8042 sets up bit serial communications with the clock/calendar chip and builds 4 time data packets. The 4 packets are converted to bytes and placed in the output buffer behind the "R" header byte. The 8042 sets up a Read Time data packet to be sent to the 8088 and returns to normal operation.

If the power fails, the calendar power status bit in the status register (Port 2FE Bit 7) is set. First, check to see if the power failure is temporary. (Perhaps the battery lost contact with the clock circuit because of a bump or jarring of the equipment.) To check for temporary failure, issue a Set Time command. If the power failure bit goes to zero everything is normal. If the power failure bit is not reset, then the battery either is dead or is dislodged from its holder clip. After replacing or resetting the battery, issue the Set Time command to ensure proper operation.

Operation of the 8042:

Upon power up/RESET, the 8042 initializes the system by zeroing all RAM and clearing all flags, ports, and registers. It then sets up the default conditions and enters the normal mouse data processing cycle, which follows:

1. The 8042 takes a copy of the Mouse/Clock/Calendar data port (P1) and saves a copy.

2. It then checks to see if there is any change in the status of the buttons. If there is, the 8042 sends a copy to the status register.

3. Next, the 8042 determines the Delta x changes or Delta y changes. Both Deltas use the same process.

4. The 8042 retrieves the copy of Port P1 and compares the bit pattern of xA and xB to the old copy to see if any changes have occured. If a change has occured, then the 8042 determines whether the change is +1, -1, or null. (Null occurs when the 8042 misses 2 state changes of xA and xB.)

5. The Delta x (or y) working accumulator (+-32735 units) is then either incremented or decremented respectively. A null result does not affect the accumulators.

6. At this point, the 8042 checks the event-triggered data polls for motion and button data. If either occurred, then the 8042 transfers the values in the working accumulators to the output buffer behind the appropriate header byte and clears the working accumulators to zero. If not, then the 8042 checks to see if any input from the 8088 has been received by checking the F1 command flag. If there is input in the input buffer, the 8042 tests the header to see which bit is "on" and jumps to the routine that handles that command.

7. After checking for input, the 8042 then checks the internal timer to see if anything has timed out. Two items are connected to the timer flag, the 8042 and the timed data transfer interrupt. All outputs to the 8088 are tied to the timer. Each time the timer times out, the 8042 checks the output register full flag to see if it is set. If the flag is set, the 8042 sends off a signal on the interrupt line to the 8088, resets the timer, and returns to normal operation. The 8042 checks to see if it needs to send any more data. If it does, it moves the next data byte to the output register, sends a signal on the interrupt line, and returns to normal operations. If the output buffer is empty, the 8042 simply returns to normal operation. Connected to the timer is the timed data transfer interrupt. When the timer interrupt is enabled, the 8042 also checks to see if the timer has timed out. If it has, then the 8042 transfers the mouse data from the working accumulators to the output buffer behind the header byte and ships it to the 8088. It then clears the working accumulators and returns to the start of the cycle.

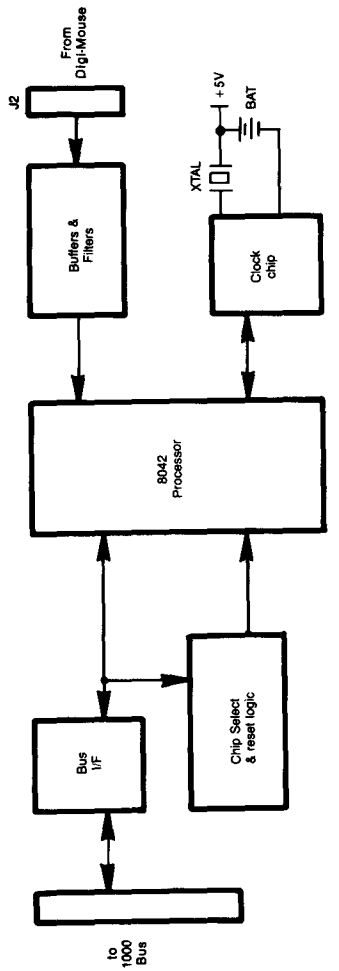


Figure 1

DIGI-Mouse/Clock Controller Board Block Diagram I/F

5/ Alignments

A Frequency Counter with a timer function is necessary for a correct alignment. To ensure an accurate time base, the trim capacitor (C19) is set at the factory. If you need to replace Y1, U8, or C19, adjust C19 for an average waveform period of 7.8125 milliseconds at Pin 11 of U8.

The oscillator will not be loaded by the test instrument because the Signetics SAB3019 Clock/Calendar chip provides a buffered oscillator output at Pin 11 that is divided by 256. The frequency at Pin 11 should be 128 Hz. Since this is a low frequency, most frequency counters are more accurate if their timer fuction is used.

No other alignments need be made. When installing the board, however, take normal precautions against static electricity discharge.

6/ Troubleshooting

If the board is malfunctioning, check to see that the clocks are present at both the 7.16MHz signal at Pin 3 of U3 and the 128Hz at Pin 11 of U8. Note: For correct operation of the clock function, the battery must have a minimum charge of 2.75 volts and make complete contact with the battery socket clip. The chip select signal at Pin 6 of U2 can be tested by using a short Basic program to access Ports 2FCh or 2FEh. Access to Ports 2FF or 2FD should generate a pulse at Pin 11 of U1. Although the inputs to CMOS (U4) are well protected, a large discharge could damage the CMOS. Swapping the processor or clock chip with known good devices can help you isolate the problem.

7/Clock/Calendar Component Side

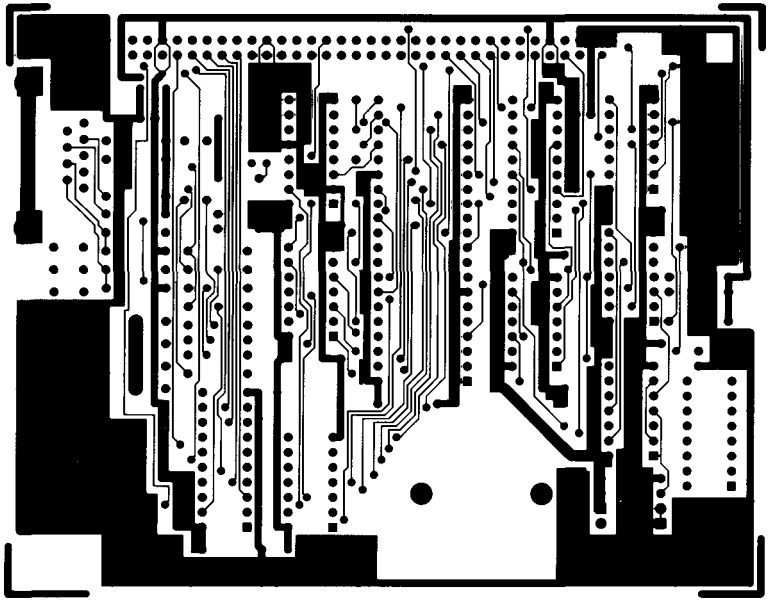


Figure 2

Clock/Calendar Solder Side

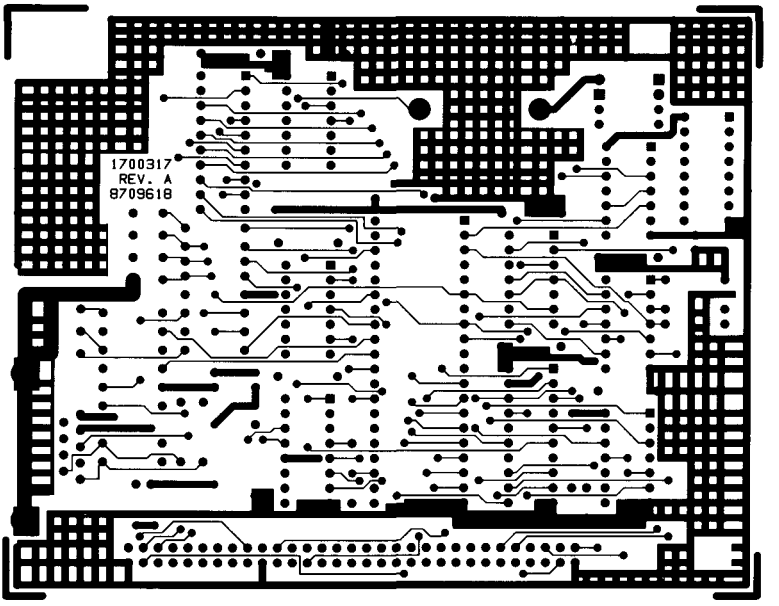


Figure 3

Clock/Calendar Silkscreen

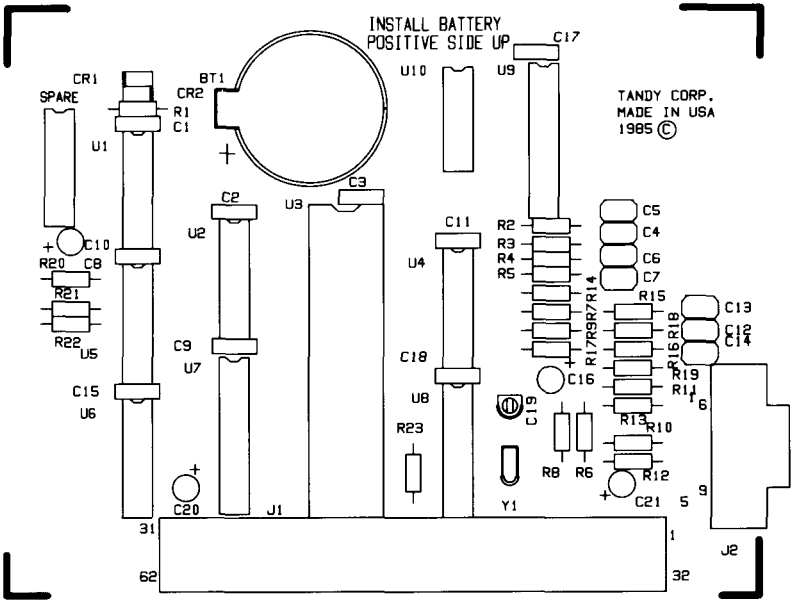
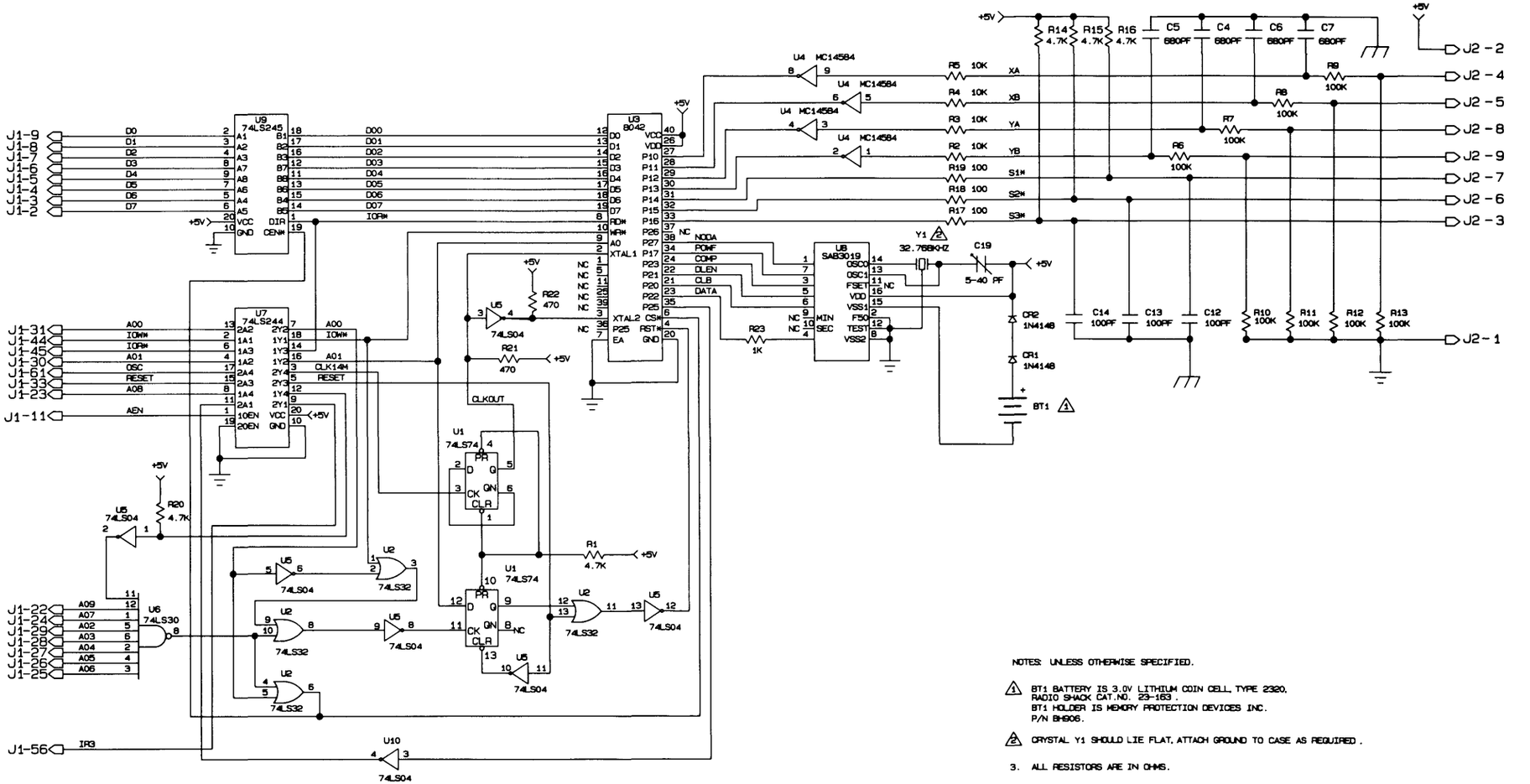


Figure 4

REVISIONS				
ZONE	LETTER	DESCRIPTION	DATE	APPROVED
	A	PRODUCTION RELEASE	8/14/85	



NOTES: UNLESS OTHERWISE SPECIFIED.

1. BT1 BATTERY IS 3.0V LITHIUM COIN CELL, TYPE 2320, RADIO SHACK CAT.NO. 23-163. BT1 HOLDER IS MEMORY PROTECTION DEVICES INC. P/N BH906.
2. CRYSTAL Y1 SHOULD LIE FLAT. ATTACH GROUND TO CASE AS REQUIRED.
3. ALL RESISTORS ARE IN OHMS.

MATERIAL	UNLESS OTHERWISE SPECIFIED		DRAFT	DATE	TITLE
	TOLERANCES		CHECK	DATE 12-21-85	SCHEMATIC, MOUSE/CALENDER-CLOCK
FINISH			DESIGN	DATE	
			APPD	DATE 12-21-85	REV. A
	DIMENSIONS ARE IN INCHES AND APPLY AFTER PLATING	642	USED ON	TANDY	DRAWING NO. 8000254
	DO NOT SCALE THIS DRAWING				SCALE - SHEET 1 OF 1

8/ **Parts List**
Tandy 1000 Mouse/Clock/Calendar
Catalog Number 25-1015

SYMBOL	QTY	DESCRIPTION	PART NO.
		DIGI MOUSE CONT./COMBO BD. REV. A	
		SCREW #4-40 X 1/4" ZINC	AHD-2991
	2	SCREWS (PANEL) #4-40 X 3/8	AHD-2222
	2	NUTS, 4-40	AHD-7166
	3	STANDOFF, NYLON PCB	AHC-2429
		STANDOFF, #4-40 HEX	AHC-2259
BT1	1	BATTERY 3.0V #23-16	ACS-0103
BT1	1	SOCKET, PCB MOUNT	AJ-7056
C1-3,8,9, 11,15,17, 18	9	CAPACITOR 0.1 MFD 50V MONO AXIAL	CC-104JJLA
C4-7	4	CAPACITOR 680 PFD 50V 20%	CC-681MJCP
C10,16, 20,21	4	CAPACITOR 33 MFD 6.3V TANTALUM RAD.	CC-336KBTP
C12-14	3	CAPACITOR 100 PFD 5% 50V	CC-101JJCP
C19	1	CAPACITOR 5-40 PFD TRIM	ACF-7370
CR1-2	2	DIODE 1N4148	DX-0022
J1	1	RECEPTACLE	AJ-4052
J2	1	CONNECTOR DB9 MALE RT. ANGLE (9-PIN) METAL SHELL, GROUNDING DETENTS AND STRAP, 4-40 THREADED INSERTS	AJ-5062
R1,14-16, 20	5	RESISTOR 4.7K OHM 1/4 WATT 5%	N-0247EEC
R2-5	4	RESISTOR 10K OHM 1/4 WATT 5%	N-0281EEC
R6-13	8	RESISTOR 100K OHM 1/4 WATT 5%	N-0371EEC
R17-19	3	RESISTOR 100 OHM 1/4 WATT 5%	N-0132EEC
R21-22	2	RESISTOR 470 OHM 1/4 WATT 5%	N-0169EEC
R23	1	RESISTOR 1K OHM 1/4 WATT 5%	N-0196EEC

SYMBOL	QTY.	DESCRIPTION	PART NO.
U1	1	IC 74LS74 FLIP FLOP	MX-3808
U2	1	IC 74LS32 QUAD 2-IN OR	MX-6183
U3	1	IC 8042 PROCESSOR	MX-6884
U3	1	SOCKET 40-PIN DIP	AJ-6580
U4	1	IC MC14584 CMOS HEX INVERTER	MX-6207
U5,10	1	IC M74LS04P HEX INVERTER	AMX-3552
U6	1	IC 74LS30 8-IN NAND	AMX-3556
U7	1	IC 74LS244 OCTAL BUS TRANSCEIVER	AMX-3864
U8	1	IC SAB3019 CAL/CLK	MX-6178
U8	1	SOCKET 16-PIN DIP	AJ-6581
U9	1	IC 74LS245 OCTAL BUFFER	AMX-4470
Y1	1	CRYSTAL 32.768 KHz.	MX-1113
Y1	1	STAKING PIN (GROUND FOR CRYSTAL)	AHB-9682

PLUS Network 4 Interface

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Theory of Operation 2

Installation Instructions 5

Parts List 11

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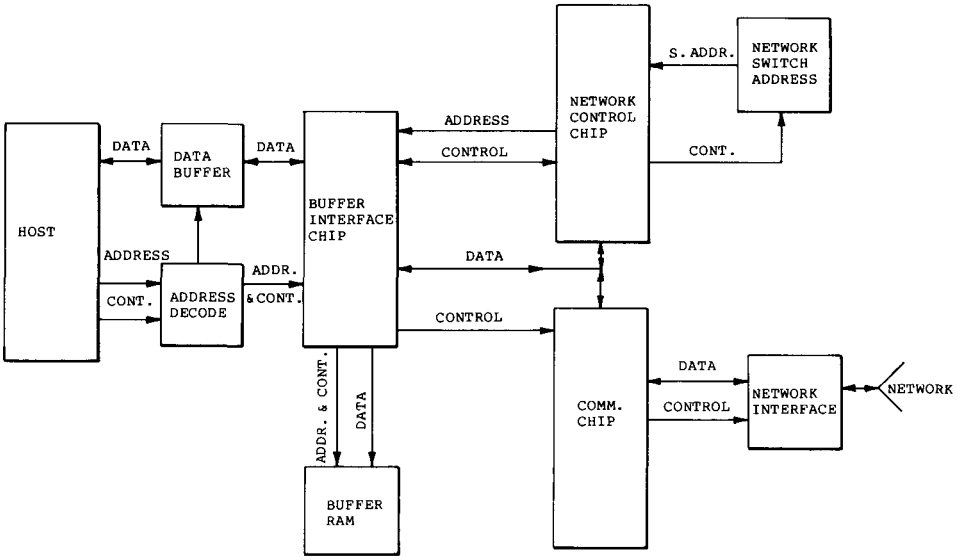
INTRODUCTION

PLUS Network 4 is Local Area Network (LAN) system for communication between as many as 64 units, all operating asynchronously at a clock rate of 1 MHz. The 64 units are tied together by twisted pairs of wires. This network is interconnected through the Tandy 1000's 62-pin option slot. This interconnection is hardwired at the I/O addresses 0248-024F, and ties the Tandy 1000 to the CORVUS chip set which does most of the data formatting and recognizes the network protocol.



THEORY OF OPERATION

Address Decode

Address decoding uses ICs U15, U16, and U17 to decode I/O port addresses. The outputs are then gated with *IOW and *IOR signals. Read and write operations are as follows:

I/O Port	Read & Write Operation
248	Read Transporter Status Byte
249	Read RAM
24A	Read the Counter Saver Byte
24B	Read RAM, Increment the Counter by 1.
248	Write the Counter High Byte
249	Write to the CAR
24A	Write the Counter Low Byte
24B	Write to RAM, Increment the Counter by 1.

Interrupt Operation

The PLUS Network 4 Interface board supports the following interrupts.

I/O Port	Interrupt Operation
24C	Disable interrupts
24D	Clear current interrupt request
24E	Enable interrupts (All three operations can be done by reading or writing with meaningless data.)
24F	Interrupt status Bit 4 set => interrupt pending Bit 5 set => interrupts disabled

Boot ROM /Buffer RAM

The PLUS Network 4 Interface board has a 2K-byte boot ROM (U11) and 4K-bytes of buffer RAM (U1, U2). ROM extends from host CPU address DF000 to address DFFFF and uses the first 1024 bytes of the 4K buffer RAM.

PLUS Network 4 Interface

The PLUS Network 4 Interface uses two components, (U10) which is a differential driver and receiver, and a transformer (T1), which acts as a filter. Note that since the input is a differential (as is the output) and the data is NRZI, which depends solely on transmission, the connector pins may be reversed on a unit without any effect to data transmission. The network interface is the lowest level of the network architecture.

Communications

The Comm. Chip, a CORVUS 68A54 Advanced Data Link Controller Chip, (U5) mainly encodes and decodes network data and monitors the network status for CRC errors, etc. This device constitutes the second level of the network architecture.

Network Control

The Network Control Chip, a CORVUS 6801 Chip, (U4) forms the network interface intelligence by monitoring the output of the Comm. chip (U5) and handling the header information. It handles the header information by communicating with the host side by a "command vector" in the buffered RAM and a message as to where to find the vector (sent via the C.A.R.). This device constitutes the third level of the network architecture.

Buffer Interface

The Buffer Interface Chip, a CORVUS 3131 Gate Array Chip, (U3) controls the timing and bus control for interfacing the users of the buffer RAM. It may be thought of as a two port memory controller, interfacing the host and the CORVUS 6801 chip with memory. In addition, the buffer interface chip also gates, times, and controls signals to each to facilitate their part of the interface.

Installation Instructions

Introduction

Adding the PLUS Network 4 Interface to your computer allows you to communicate with up to 64 units, all operating asynchronously at 1 MHz., via the Network 4 LAN (local area network).

The PLUS Network 4 Interface is readily installable by you. However, you can have the kit installed by the service technicians at your Radio Shack Service Center. Having service technicians install the kit not only ensures expert installation, but also enables them to quickly check that all the equipment is functioning properly.

Installation

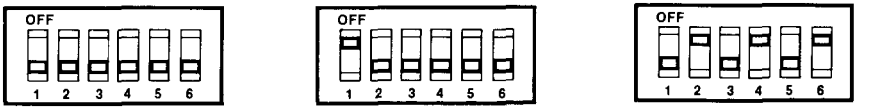
Caution should be exercised in low humidity environments to prevent damage to electronic parts by static electricity being discharged through them. Discharge any built-up static electricity by touching a grounded metal object before proceeding further.

Warning: Turn off all equipment. Turn the power off and disconnect the power cord from the wall socket. If the computer is on, you could damage the central processing unit, as well as your PLUS Network 4 Interface board.

Before proceeding with the installation of the PLUS Network 4 Interface, be sure the kit contains the PLUS Network 4 Interface board, a terminal block and 2 star washers, 2 wing nuts, an alternate mounting bracket and 2 mounting screws, and 3 plastic standoffs (for the Tandy 1000 SX).

On the PLUS Network 4 Interface board locate the jumper at J1 which selects the interrupt that is to be used. Be sure the jumper is set to interrupt 3 (IR3) as this interrupt is recognized by the software.

Also on the PLUS Network 4 Interface board, find DIP Switch SW1 (in the mounting bracket) which selects the station number. The settings on the DIP switches are a binary encoding of the numbers 0 to 63 (decimal). Each dip switch represents a digit in the 6 bit binary number. A switch set to down or "OFF" equals bit on or binary "1". Switch SW1-1 is the least significant bit. See the switch setting examples in Figure 1.



Station 0 Station 1 Station 42

Figure 1.

Note: On each PLUS Network 4 Interface board set these SW1 switches to a **unique number** of 0-63. **Be sure to record the switch settings for each computer.** The software currently selects station 63 as the disk server, therefore, we recommend that the stations be set at 0-62.

If the PLUS Network 4 Interface board is going to be installed in the Tandy 1000 EX:

1. Slide the cover on the top of the left side of the computer toward the back and remove it. See Figure 2.

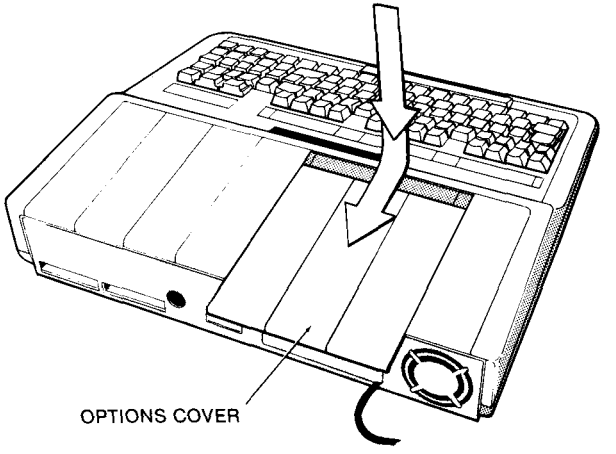


Figure 2.

2. Remove the option slot panel. If necessary break off a panel for an unused expansion slot.

3. Carefully install the PLUS Network 4 Interface board in the empty expansion slot by aligning the pins and the connector and pressing the PLUS Network 4 Interface board down firmly but gently to seat it either in the main logic board or the lower connector of the Memory PLUS Expansion Adapter. See Figure 3.

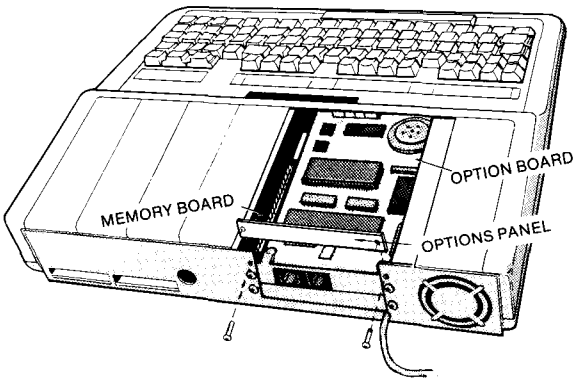


Figure 3.

4. Secure the metal mounting bracket on the PLUS Network 4 Interface board to the chassis with the screws provided.

5. Slide the terminal block over the 2 screws that protrude from the back of the computer, with the flat side of the block with 2 round indentations facing to the outside. See Figure 4.

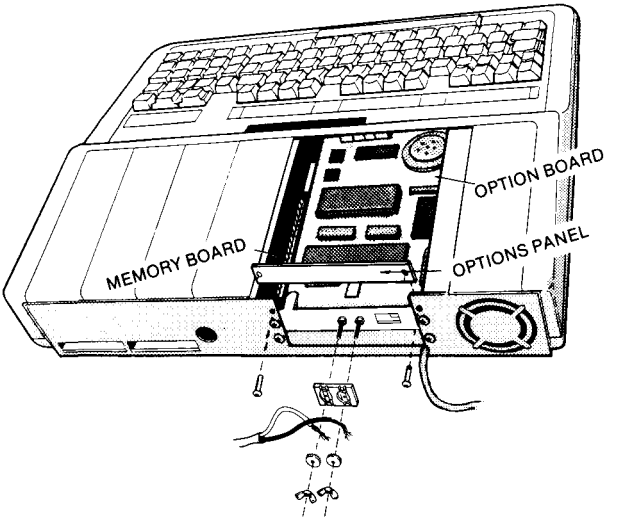


Figure 4

6. Slip the 2 star washers over the protruding screws, with the teeth facing toward the terminal block. Also install the 2 wing nuts on the ends of the screws.

7. Install a strand of the network cable between the terminal block and the star washer on one of the protruding screws and tighten the wing nut. Do likewise for the other cable strand, protruding screw and wing nut.

8. Insert the cover on the top of the left side of the computer and slide it forward toward the front. See Figure 5.

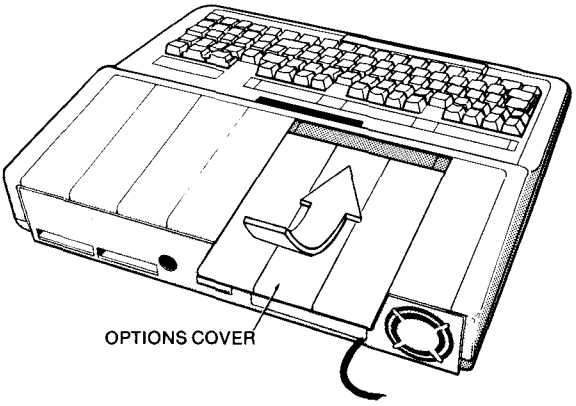


Figure 5.

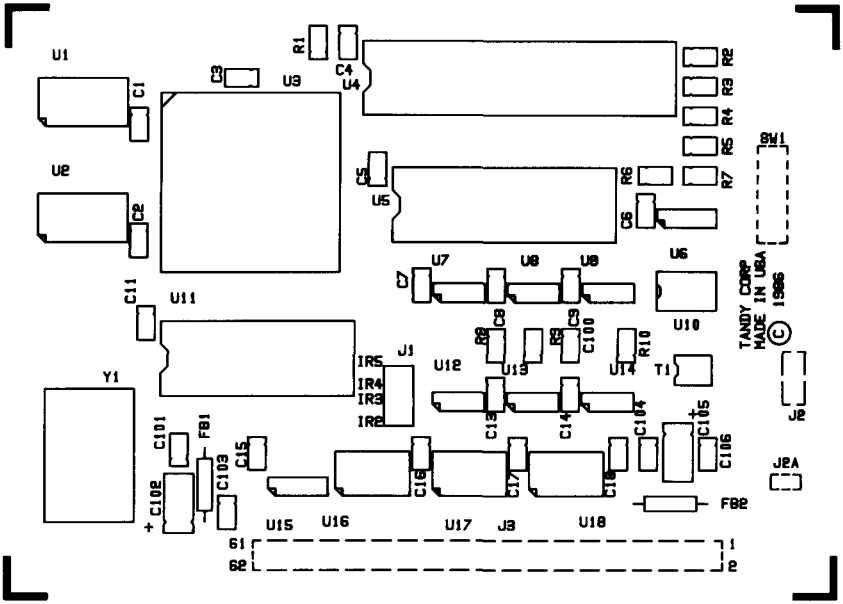
The PLUS Network 4 Interface is now ready for use. See the PLUS Network 4 Interface Owner's Manual.

TANDY 1000 Network SMT Parts List

Symbol	Description	Part No.
	PC Board, T1000 Network SMT	8859002A
C1-9,11,13-18, 101,103,104,106	Capacitor 0.1 MFD 50V Axial	X37410341
C102,105	Capacitor 33 MFD 10V Tant.Rad.	X33633310
C100	Capacitor 220 PFD	X30122241
FB1,2	Ferrite Bead	8419013
J1	Staking Pin	8529014
J2	Connector 2-Pos. Rt. Angle	8519308
J3	Connector, Recepticle 2 X 31	8519257
R1	Resistor 3K Ohm 1/8W 5%	X20323030
R2-7	Resistor 22K Ohm 1/8W 5%	X20332230
R8,10	Resistor 2.2K Ohm 1/8W 5%	X20322230
R9	Resistor 1K Ohm 1/8W 5%	X20321030
SW1	Switch, 12-Pin 6 POS DIP Rt. Angle	8489087
T1	Transformer	8417001
U1,2	SOWIC, 4016 2KX8 Static RAM	X04016020
U3	IC, Corvus Chip Set #2 (3131)	8075131
U3	Socket 68-Pin	8509020
U4	IC, Corvus Chip Set #3 (MC6801)	8075801
U4	Socket 40-Pin	8509002
U5	IC Corvus Chip Set #1 (MC6854)	8075054
U5	Socket 28-Pin	8509007
U6	SOIC, 74LS367	X02367000
U8	SOIC, 74LS125	X02125000
U7	SOIC, 74LS08	X02008000
U9	SOIC, 74LS04	X02004000
U10	IC, SN75176	8050176
U11	IC, TMS2732A 300NS	8040732
U11	Socket 24-Pin	8509001
U12	SOIC, 74LS21	X02021000
U13	SOIC, 74LS32	X02032000
U14	SOIC, 74LS74	X02074000
U15	SOIC, 74LS138	X02138000
U15	Socket 8-Pin	8509011
U16,17	SOWIC, 74LS688	X02688000
U18	SOWIC, 74LS245	X02245000
Y1	Oscillator, 10 MHz	8409041

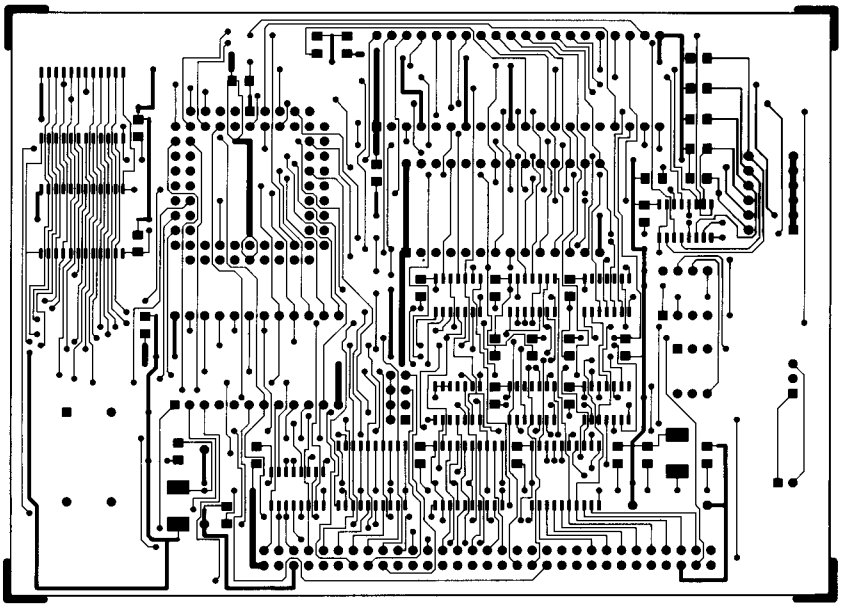
TANDY 1000 Network SMT Parts List

Symbol	Description	Part No.
	Bracket,	8729601
	Bracket,	8729572
	Standoff, Pastic	8590164



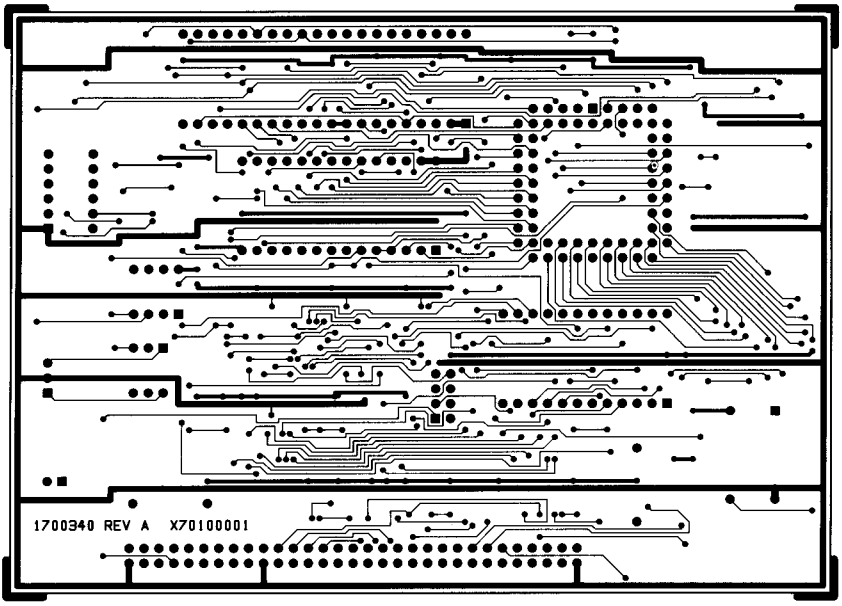
TANDY SYSTEMS DESIGN FILMWORK	FAB. SPEC.: TSD-C262-2
PROJECT NO.: 804 DATE: 06/17/86	C/S SILKSCREEN
TITLE: NETWORK	
DWG. NO.: 1700340 REV. A	
PART NO.: X7010000!	
DESIGN GRID: x=.025 y=.025	
DESIGNER: GM DD	
INSP	

PLUS Network 4 Interface Board - Silkscreen



TANDY SYSTEMS DESIGN FILMWORK		FAB. SPEC.: TSD-C262-2
PROJECT NO.: 804	DATE: 06/17/86	
TITLE: NETWORK		
DWG. NO.: 1700340	REV. A	
PART NO.: X70100001		LAYER 1 COMPONENT SIDE
DESIGN GRID: x=.025	y=.025	
DESIGNER: GM DD		
INSP		

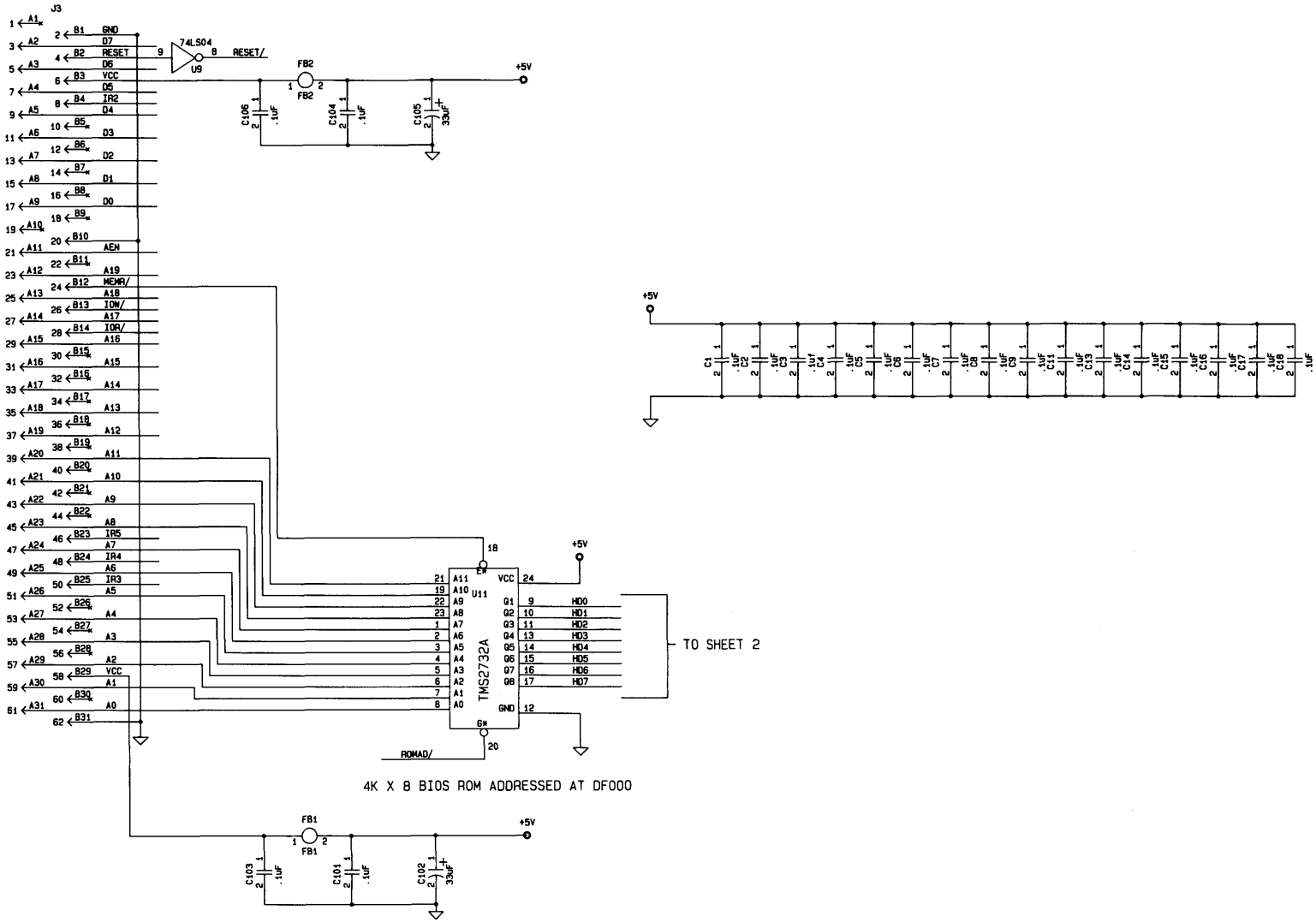
PLUS Network 4 Interface Board - Component Side



TANDY SYSTEMS DESIGN FILMWORK	FAB. SPEC.: TSD-C262-2
PROJECT NO.: 804 DATE: 06/17/86	LAYER 2 SOLDER SIDE
TITLE: NETWORK	
DWG. NO.: 1700340 REV. A	
PART NO.: X70100001	
DESIGN GRID: x=.025 y=.025	
DESIGNER: GM DD	
INSP	

PLUS Network 4 Interface Board - Solder Side

REVISION				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	RELEASE FOR PRODUCTION	7/15/86	



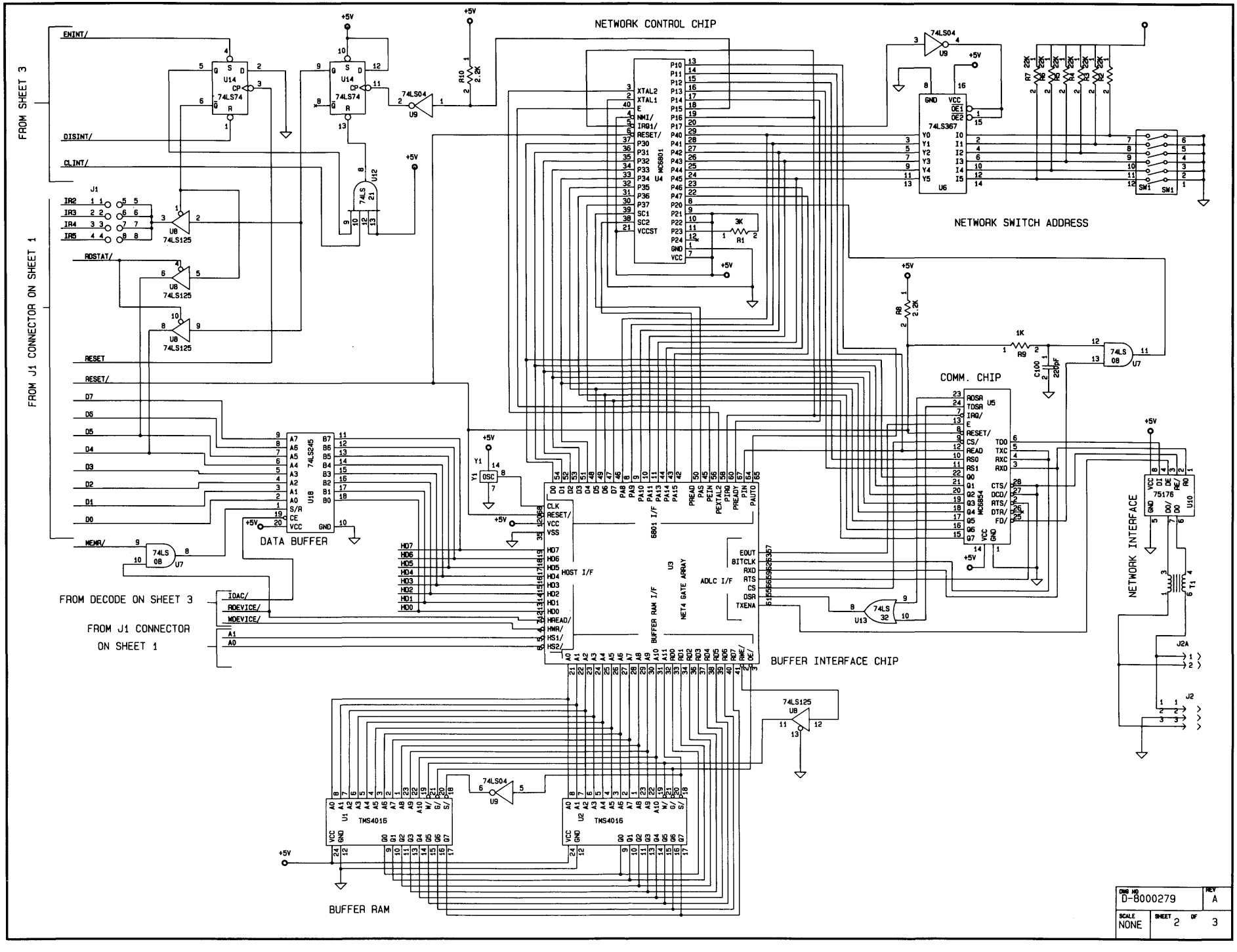
4K X 8 BIOS ROM ADDRESSED AT DF000

NOTE: THE FOLLOWING SIGNALS CONNECT TO PAGE 2 & 3. D0-D7, A0-A19, HD1-HD8, RESET/, AEN, MEMR/, IOR/, IOW/, IR2-IR5.

NOTE: THIS IS A CAD GENERATED DRAWING - DO NOT REVISE MANUALLY.

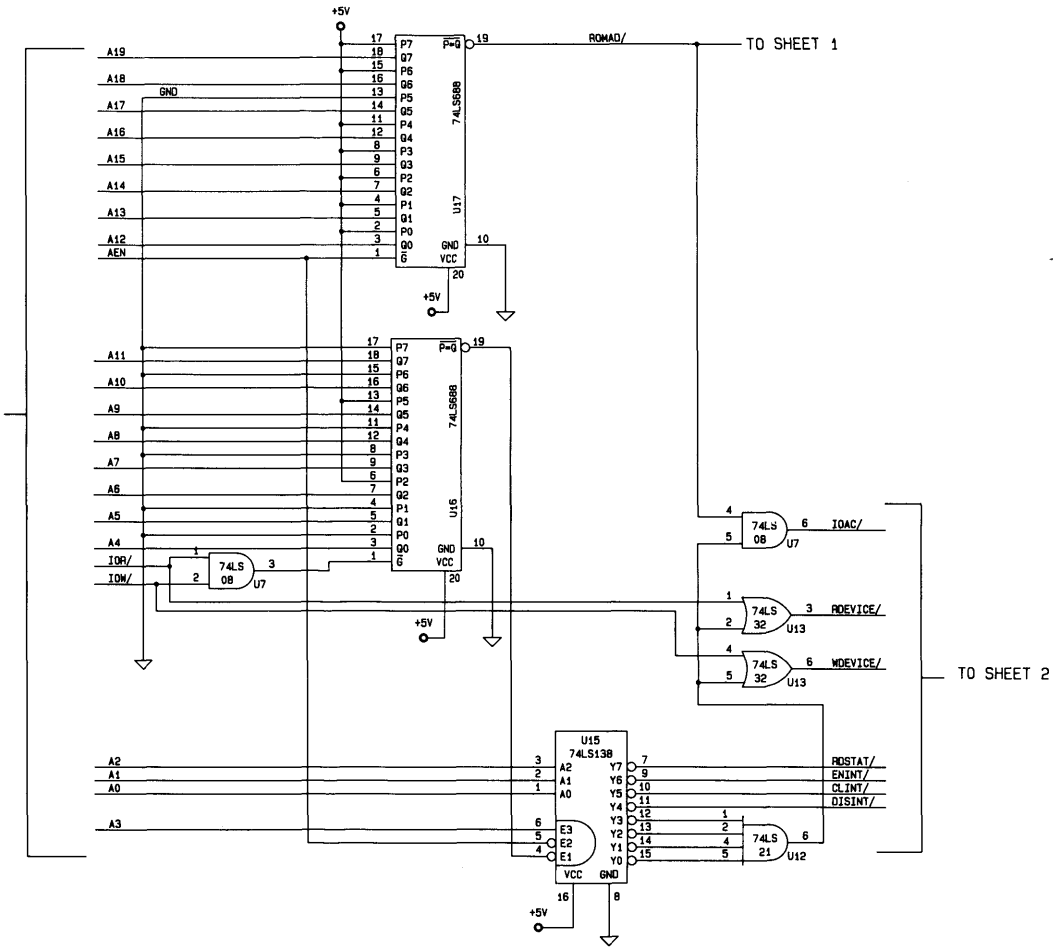
648

DRAFT N.J.	DATE 7-15-86	TITLE	SCHEMATIC
CHECK	DATE 7-14-86		NETWORK 4
DESIGN N. Jarrah	DATE 7-15-86		TANDY 1000
APPD	DATE 7-15-86	REV	A
APPD	DATE 7/15/86	DWG NO	D-8000279
TANDY		SCALE	SHEET 1 OF 3


NETWORK CONTROL CHIP
NETWORK SWITCH ADDRESS
COMM. CHIP
NETWORK INTERFACE
DATA BUFFER
BUFFER INTERFACE CHIP
BUFFER RAM
FROM SHEET 3
FROM J1 CONNECTOR ON SHEET 1
FROM DECODE ON SHEET 3
FROM J1 CONNECTOR ON SHEET 1
ENINT/
DISINT/
CLINT/
RDSTAT/
RESET
RESET/
D7
D6
D5
D4
D3
D2
D1
D0
MEMR/
IOAC/
RDEVICE/
WDEVICE/
A1
A0
HD7
HD6
HD5
HD4
HD3
HD2
HD1
HD0
MREAD/
MWR/
HS1/
HS2/
6801 I/F
HOST I/F
BUFFER RAM I/F
NET4 GATE ARRAY
ADLC I/F
EOUT
BITCLK
RXD
RTS
CS
DSR
TXENA
74LS74
74LS04
74LS125
74LS367
74LS245
74LS 08
74LS 32
MC6801
MC6854
75176
TMS4016
DWG NO
D-8000279
REV
A
SCALE
NONE
SHEET
2
OF
3

	A19	A16	A15	A12	A11	A8	A7	A4	A3	A0	
ROM	1101	1111	XXXX	XXXX	XXXX						(DF000)
	1100	0000	XXXX	XXXX	XXXX						(C0000)
I/O	XXXX	XXXX	0010	0100	0XXX						(240)
	XXXX	XXXX	0010	0100	1XXX						(248)
	XXXX	XXXX	0011	0110	0XXX						(360)
	XXXX	XXXX	0011	0110	1XXX						(368)
	110A	AAAA	XXXX	XXXX	XXXX						TWO ADDRESSES
	XXXX	XXXX	001I	01I0	SDDD						FOUR ADDRESSES

X = DON'T CARE
A = ROM CHANGES 1 TO 0
I = I/O CHANGES 0 TO 1
S = STEP UP 8
D = DECODE ADDRESS



DWG NO	REV
D-8000279	A
SCALE	SHEET 3 OF 3

DEVICES

DEVICES
CONTENTS

VIDEO CONTROLLER CHIP SPECIFICATION
DMA CHIP SPECIFICATION
PRINTER INTERFACE
KEYBOARD INTERFACE
TIMING CONTROL GENERATOR

VIDEO CONTROLLER CHIP SPECIFICATION

VIDEO CONTROLLER CHIP SPECIFICATION
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BLOCK DIAGRAM.....2
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ELECTRICAL SPECIFICATIONS.....29
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VIDEO CONTROLLER CHIP SPECIFICATION

GENERAL DESCRIPTION

The Tandy 1000 video controller chip is designed to operate with three types of display devices: A standard TV using an RF modulator, a composite monitor, and an RGBI 200 line Color monitor. This custom controller chip implements all of the video logic for the Tandy 1000 plus most of the system decode logic. Figure 1 shows a block diagram of the controller chip.

The video display system is very flexible and can be programmed for a number of video modes. These modes use varying numbers of colors (2,4 or 16). These 16 colors are defined by combinations of the RGBI as shown in the color chart below and can be used for the foreground color or background color. If you are using a black and white monitor, these colors will appear as shades of gray. In addition, any 1 of the 16 colors or shades of gray can be used for the screen border.

I	R	G	B	Color
0	0	0	0	Black
0	0	0	1	Blue
0	0	1	0	Green
0	0	1	1	Cyan
0	1	0	0	Red
0	1	0	1	Magenta
0	1	1	0	Brown
0	1	1	1	Light Gray
1	0	0	0	Dark Gray
1	0	0	1	Light Blue
1	0	1	0	Light Green
1	0	1	1	Light Cyan
1	1	0	0	Pink
1	1	0	1	Light Magenta
1	1	1	0	Yellow
1	1	1	1	White

TABLE 1 AVAILABLE COLORS TABLE

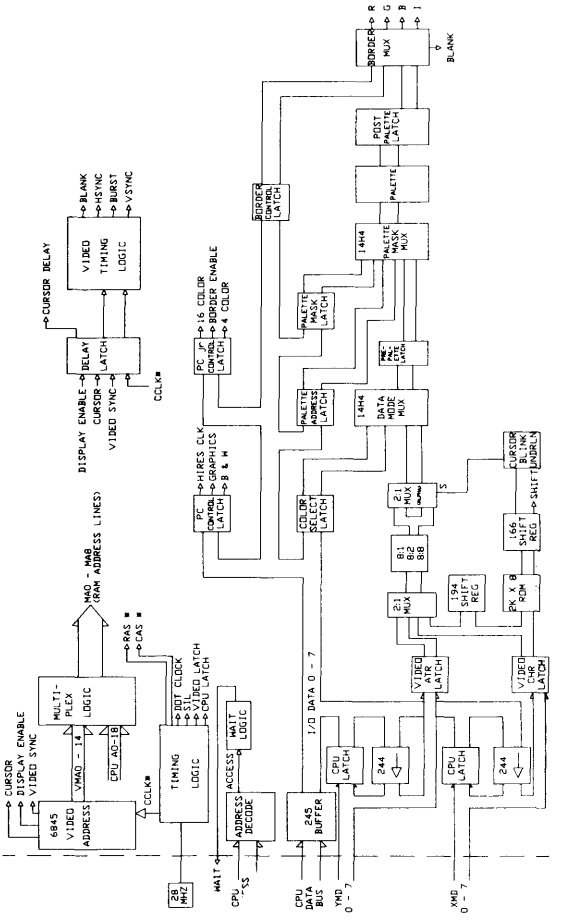


Figure 1. VIDEO CONTROLLER CHIP BLOCK DIAGRAM

OPERATING MODES

The operating modes supported by the Tandy 1000 video controller may be grouped in two categories: Alphanumeric and Graphic.

ALPHANUMERIC MODE

The Alphanumeric mode has two basic types of operation: 80 character by 25 rows, and 40 character by 25 rows. In both modes the characters are generated by a 256 character ROM. The character ROM is divided into the following groups:

* 96 Standard ASCII characters
* 48 Block Graphics characters
* 64 Foreign Language/Greek characters
* 16 Special Graphics characters.
* 32 Word Processing/Scientific Notation characters

In both modes all characters are 7 dots wide by 7 dots high and are placed in an 8 dot wide by 8 or 9 dot high matrix. In both the 40x25 and the 80x25 modes, two bytes of data are used to define each character on the screen. The even address (0,2,4 etc.) is the character code and is used in addressing the character generating ROM. The odd address (1,3,5 etc.) is the attribute byte, that defines the foreground and the background color of the character. The following chart shows how the attribute byte controls colors.

ATTRIBUTE BYTE							
7	6	5	4	3	2	1	0
Background				Foreground			
I	R	G	B	I	R	G	B
.	R	G	B	I	R	G	B

+---> =1 Selects Blinking of foreground if enabled

Table 2 ALPHANUMERIC MODE ATTRIBUTE BYTE DEFINITION

* Writing a 1 in bit 5 of register 'H3D8 enables Blinking

GRAPHICS MODE

The Tandy 1000 Video Controller chip can be programmed for a variety of modes.
The Tandy 1000 Computer family supports the following Graphics Modes:

MODE		IBM PCJR	IBM PC
4 Color Medium Resolution	320 x 200	X	X
16 Color Medium Resolution	320 x 200	X	
16 Color Low Resolution	160 x 200	X	
2 Color High Resolution	640 x 200	X	X
4 Color High Resolution	640 x 200	X	

GRAPHICS MEMORY USAGE

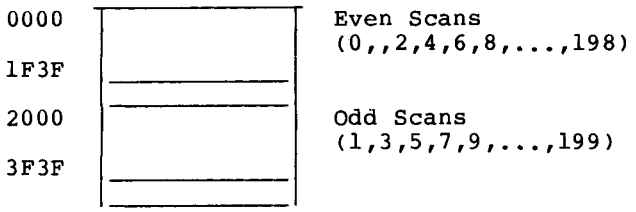
* 200 line Graphics Memory uses either 2 or 4 banks of 8000 bytes. In either case, pixel information for the display's upper left corner is found at address 0000.

```
####   The  4 Color High Resolution 640 X 200 and
####   The 16 Color Medium Resolution 640 X 200
####   use 4 banks of 8000 bytes as follows

(Hex) | <------160 Bytes------>

0000  ┌──────────────────────┐   00 Scans
      │                      │   (0,4,8,...,196)
1F3F  ├──────────────────────┤
      ├──────────────────────┤
2000  │                      │   01 Scans
      │                      │   (1,5,9,...,197)
3F3F  ├──────────────────────┤
      ├──────────────────────┤
4000  │                      │   10 Scans
      │                      │   (2,6,10,...,198)
5F3F  ├──────────────────────┤
      ├──────────────────────┤
6000  │                      │   11 Scans
      │                      │   (3,7,11,...,199)
7F3F  ├──────────────────────┤
      └──────────────────────┘
```

```
####   The  2 Color High Resolution 640 X 200 and
####   The  4 Color Medium Resolution 640 X 200 and
####   The 16 Color Low Resolution 640 X 200
####   use only 2 banks of 8000 bytes as follows
```



2 COLOR HIGH RESOLUTION 640 X 200 GRAPHICS MODE

The 2 Color High Resolution 640 X 200 Graphics mode may require a high resolution monitor for proper operation. Available in the IBMPC and IBM PCjr, this mode has the following characteristics:

Contains a maximum of 200 rows of 640 PELs
Can display 2 of 16 possible colors
Requires 16K bytes of read/write memory
Formats 8 PELs per byte for each byte in the following manner:

7	6	5	4	3	2	1	0
PA3	PA2	PA1	PA0	PA3	PA2	PA1	PA0
First Display PEL	Second Display PEL	Third Display PEL	Fourth Display PEL	Fifth Display PEL	Sixth Display PEL	Seventh Display PEL	Eighth Display PEL

4 COLOR HIGH RESOLUTION 640 X 200 GRAPHICS MODE

The 4 Color High Resolution 640 X 200 Graphics mode may require a high resolution monitor for proper operation. Only supported on the IBM PCjr, this mode has the following characteristics:

Contains a maximum of 200 rows of 640 PELs
Can display 4 of 16 possible colors
Each pixel selects 1 of 4 colors
Requires 32K bytes of read/write memory
Formats 8 PELs per two bytes (1 even byte and 1 odd byte) in the following manner:

EVEN BYTES

7	6	5	4	3	2	1	0
PA0	PA0	PA0	PA0	PA0	PA0	PA0	PA0
First Display PEL	Second Display PEL	Third Display PEL	Fourth Display PEL	Fifth Display PEL	Sixth Display PEL	Seventh Display PEL	Eighth Display PEL
PA1	PA1	PA1	PA1	PA1	PA1	PA1	PA1
7	6	5	4	3	2	1	0

ODD BYTES

16 COLOR MEDIUM RESOLUTION 320 X 200 GRAPHICS MODE

The 16 Color Medium Resolution 320 X 200 Graphics mode works with all types of display devices. This mode is available in the IBM PCjr only and has the following characteristics:

Contains a maximum of 200 rows of 320 PELs
Can display 16 of 16 possible colors
Each pixel selects 1 of 16 colors
Requires 32K bytes of read/write memory
Formats 2 PELs per byte in the following manner:

7	6	5	4	3	2	1	0
PA3	PA2	PA1	PA0	PA3	PA2	PA1	PA0
First Display PEL				Second Display PEL			

16 COLOR LOW RESOLUTION 160 X 200 GRAPHICS MODE

The 16 Color Low Resolution 160 X 200 Graphics mode works with all types of display devices. This mode is available in the IBM PCjr only, with the following characteristics:

Contains a maximum of 200 rows of 160 PELs
Can display 16 of 16 possible colors
Each pixel selects 1 of 16 colors
Requires 16K bytes of read/write memory
Formats 2 PELs per byte in the following manner:

7	6	5	4	3	2	1	0
PA3	PA2	PA1	PA0	PA3	PA2	PA1	PA0
First Display PEL				Second Display PEL			

4 COLOR MEDIUM RESOLUTION 320 X 200 GRAPHICS MODE

The 4 Color Medium Resolution 320 X 200 Graphics mode works with all types of display devices. It is available in the IBM PC and PCjr. This mode has the following characteristics:

Contains a maximum of 200 rows of 320 PELs
Can display 4 of 16 possible colors
Each pixel selects 1 of 4 colors
Requires 16K bytes of read/write memory
Formats 4 PELs per byte in the following manner:

7	6	5	4	3	2	1	0
PA1	PA0	PA1	PA0	PA1	PA0	PA1	PA0

First Display PEL	Second Display PEL	Third Display PEL	Fourth Display PEL

VIDEO MEMORY MAP AND GRAPHICS USAGE

Hex Address	Register
3D0	Not Used
3D1	Not Used
3D2	Not Used
3D3	Not Used
3D4	G845 Address Register
3D5	G845 Data Register
3D6	Not Used
3D7	Not Used
3D8	Mode Select Register
3D9	Color Select Register
3DA	Video Array Address & Status
3DB	Clear Light Pen Latch
3DC	Set Light Pen Latch
3DD	Extended RAM Page Register
3DE	Video Array Data
3DF	CRT Processor Page Register

VIDEO ARRAY REGISTERS

The following registers can be accessed by writing their Hex Address to 3DA and their Data to 3DE

Hex Address	Video Array Register
01	Palette Mask
02	Border Color
03	Mode Control
10-1F	Palette Registers

ARRAY PALETTE MASK REGISTER

Bit Programming

Hex Address	Array Register	7	6	5	4	3	2	1	0	Notes
01	Palette Mask	X	X	X	X					Write Only
MSK[3]	Palette Mask 3									
MSK[2]	Palette Mask 2									
MSK[1]	Palette Mask 1									
MSK[0]	Palette Mask 0									

When bits 0-3 are 0, they force the appropriate palette address to be 0 regardless of the incoming color information. This can be used to make some information in memory a 'don't care' condition until it is requested.

ARRAY BORDER COLOR

Hex Address	Array Register	7	6	5	4	3	2	1	0	Notes
02	Border Color	X	X	0	X					Write Only
	Reserved = 0									
BORI	I (Intensity) Border Color Select									
BORR	R (Red) Border Color Select									
BORG	G (Green) Border Color Select									
BORB	B (Blue) Border Color Select									
	A combination of bits 0-3 selects the screen border as one of 16 colors, as listed in Table 1 "Available Colors Table" at the beginning of this section.									

ARRAY MODE CONTROL REGISTER

Hex Address	Array Register	Bit Programming 7	6	5	4	3	2	1	0	Notes
03	Mode Control	X	X					0	X	Write Only
NVDM	Set to 1 for 640x200 secondary pixel organization									
C16COL	Set to 1 for 16 Color Modes									
C4COLHR	Set to 1 for 4 Color 640x200 Mode									
BORENB	Enables the border color register. For PC compatibility, this bit should be 0. For PCjr compatibility, this bit should be 1.									
	Reserved for future implementations. Must always be set to zero.									

ARRAY PALETTE REGISTERS

There are sixteen 4 bit wide palette registers implemented by a 16x4 bit RAM. These registers are 'write' only; they cannot be 'read'. Their address in the Video Array are from hex 10 to 1F. They can be used to redefine any color.

To load the palette, write the hex address to the Video Array register at 3DA. Then, the new palette color is written to 3DE.

Palette address hex 10 is accessed whenever the color code from memory is a hex 0, address hex 11 is accessed whenever the color code from memory is a hex 1, and so forth. A description of the color codes is in Table 1 "Available Colors Table" at the beginning of this section.

Note: The palette address can be 'masked' by using the palette mask register.

The following is a description of the register's bit functions:

Bit Number	Function
0	Blue
1	Green
2	Red
3	Intensity

When loading the palette, the video is 'disabled' and the color viewed on the screen is the data contained in the register being addressed by the processor.

When the program has completed loading the palette, it must change the hex address to some address less than hex 10 for video to be 'enabled' again.

If a programmer does not wish a user to see the adverse effects of loading the palette, the palette should be loaded during the vertical retrace time. The program must modify the palette and change the address to less than hex 10 within the vertical retrace time. A vertical retrace interrupt and a status bit are provided to facilitate this procedure.

In two color modes, the palette is defined by using one bit (PA0), with the following logic:

PALETTE ADDRESS BIT

PA0	Function
0	Palette Register 0
1	Palette Register 1

In four color modes, the palette is defined by using two bits (PA1 and PA0), with the following logic:

PALETTE ADDRESS BITS

PA1	PA0	Function
0	0	Palette Register 0
0	1	Palette Register 1
1	0	Palette Register 2
1	1	Palette Register 3

In sixteen color modes, the palette is defined by using four bits (PA3,PA2,PA1 and PA0), with the following logic:

PALETTE ADDRESS BITS

PA3 (I)	PA2 (R)	PA1 (G)	PA0 (B)	Function
0	0	0	0	Palette Register 0
0	0	0	1	Palette Register 1
0	0	1	0	Palette Register 2
0	0	1	1	Palette Register 3
0	1	0	0	Palette Register 4
0	1	0	1	Palette Register 5
0	1	1	0	Palette Register 6
0	1	1	1	Palette Register 7
1	0	0	0	Palette Register 8
1	0	0	1	Palette Register 9
1	0	1	0	Palette Register 10
1	0	1	1	Palette Register 11
1	1	0	0	Palette Register 12
1	1	0	1	Palette Register 13
1	1	1	0	Palette Register 14
1	1	1	1	Palette Register 15

DETAILED I/O REGISTER INFORMATION

Bit Programming

Hex Address	Register	7	6	5	4	3	2	1	0	Notes
3D4	6845 Address Register	X	X	X						Write Only
					<- 5 bit address ->					Addresses 1 of 18 6845 Registers
Hex Address	Register	7	6	5	4	3	2	1	0	Notes
3D5	6845 Data Register									Write Only
		<------ 8 bit Data ---->								Data placed in 1 of 18 6845 Registers

Bit Programming

Hex Address	Register	7	6	5	4	3	2	1	0	Notes
3D8	Mode Register	X	X							Write Only
ENABLINKCR	Alpha Blink Enable.A 1 selects blink if attribute bit 7 is set. A 0 selects 16 background colors. A 1 selects 8 background colors.									
HRESAD	640 Dot Graphics. A 1 selects 640 X 200 (2 or 4 Color)									
VIDENBCR	Video Enable. A 1 enables the Video display.									
BW	Black & White Select. Selects B&W or color mode for TV or composite monitors. In RGB monitors, a different color palette is selected by this bit in 320 x 200 4 Col Mode. This bit will have no other effect on RGB operation									
GRPH	Graphics Select. A 0 selects Alpha-numeric Mode. A 1 selects Graphics Mode.									
HRESCK	High Resolution Dot Clock. A 0 selects the lower speed for 40 character text or low resolution graphics mode. A 1 selects the higher speed for 80 character text or high resolution graphics mode.									

Bit Programming

Hex Address	Register	7	6	5	4	3	2	1	0	Notes
3D9	Color Select Register	X	X							Write Only
COLSEL	320 X 200 4 Color Blue Control									
BACKGROUNDI	Alpha Background/320 Graphics Foreground Intensity. When Blink is enabled in alpha mode, this bit is used to select intensity. In the 320 X 200 4 color mode, it selects the intensity of the foreground									
OVERSCANI	In Alpha mode screen Border intensity In 320x200 4 Col Background intensity if PA0=PA1=0 In 640x200 2 Col Foreground intensity									
OVERSCANR	In Alpha mode screen Border Red In 320x200 4 Col Background Red if PA0=PA1=0 In 640x200 2 Col Foreground Red									
OVERSCANG	In Alpha mode screen Border Green In 320x200 4 Col Background Green if PA0=PA1=0 In 640x200 2 Col Foreground Green									
OVERSCANB	In Alpha mode screen Border Blue In 320x200 4 Col Background Blue if PA0=PA1=0 In 640x200 2 Col Foreground Blue									

Bit Programming

Hex Address	Register	7	6	5	4	3	2	1	0	Notes
3DA	Video/Light Pen Status	X	X	X	X					Read Only
CVSYNC	When 1 Vertical retrace is active									
LPSWB	Light Pen Switch Status When 0 Light Pen Switch is on. Switch not latched or debounced.									
LPSTRB	When 1 Light Pen input has positive going edge and has set Light Pen trigger. When this trigger is low during a system power on, it may be cleared by performing an I/O command to address 3DB. No specific data is required.									
DISPENB	When 0 Display is active When 1 Video is not displayed									

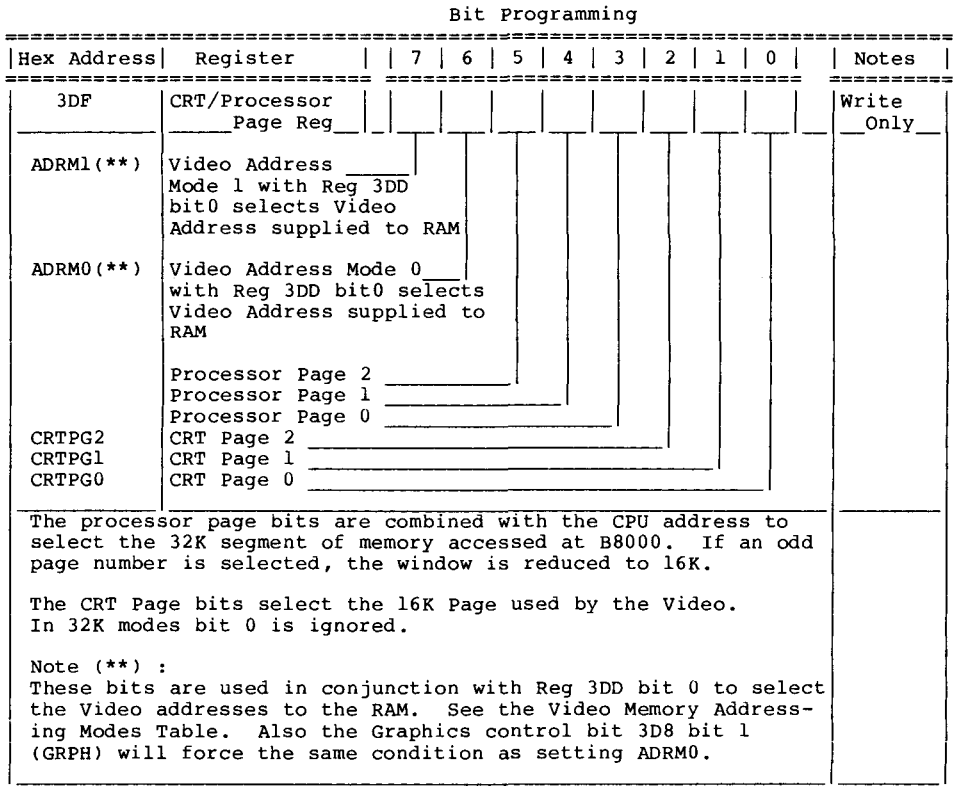
Bit Programming

Hex Address	Register	7	6	5	4	3	2	1	0	Notes
3DC	Set Light Pen Latch	X	X	X	X	X	X	X	X	Write Only
3DB	Clear Light Pen Latch	X	X	X	X	X	X	X	X	Write Only
	Data Byte has no effect. Before the 6845 can read the light pen again, the latch at 3DB must be cleared									

Bit Programming

Hex Address	Register	7	6	5	4	3	2	1	0	Notes
3DD	Extended Ram Page Reg	X					X	X		Write Only
PG18 (#)	CPU Page Address 18									All bits cleared by a System Reset
PG17	CPU Page Address 17									
VPG18 (#)	Video Page Address 18									
VPG17	Video Page Address 17									
EXTADR	Extended Addressing Mode for 256K systems									

Note (#) Not implemented in current design but reserved for future implementations


Bit Programming
Hex Address
Register
7
6
5
4
3
2
1
0
Notes
3DF
CRT/Processor Page Reg
Write Only
ADRM1(**)
Video Address Mode 1 with Reg 3DD bit0 selects Video Address supplied to RAM
ADRM0(**)
Video Address Mode 0 with Reg 3DD bit0 selects Video Address supplied to RAM
Processor Page 2
Processor Page 1
Processor Page 0
CRTPG2
CRT Page 2
CRTPG1
CRT Page 1
CRTPG0
CRT Page 0
The processor page bits are combined with the CPU address to select the 32K segment of memory accessed at B8000. If an odd page number is selected, the window is reduced to 16K.
The CRT Page bits select the 16K Page used by the Video. In 32K modes bit 0 is ignored.
Note (**) :
These bits are used in conjunction with Reg 3DD bit 0 to select the Video addresses to the RAM. See the Video Memory Addressing Modes Table. Also the Graphics control bit 3D8 bit 1 (GRPH) will force the same condition as setting ADRM0.

Bit Programming

Hex Address	Register	7	6	5	4	3	2	1	0	Notes
00A0-00A7	NMI Mask Register		X	X						Write Only
NMIEN	Enable Non Maskable Interrupt									
PORTMD	Enable 256K Video RAM									All bits
MC3	Memory Configuration 3									cleared
MC2	Memory Configuration 2									by a
MC1	Memory Configuration 1									System
XTERNVID	Disables all video Accesses to Video Memory at B8000-BFFFF and video I/O locations 3D0-3D7									Reset

6845 PROGRAMMING TABLE FOR ALL MODES

*	REGISTER	40X25 ALPHANUM	80X25 ALPHANUM	160X200 16 Col 320X200 4 Col 640X200 2 Col	640X200 4 Col 320X200 16 Col
0	Horizontal Total	38 (56)	71 (113)	38 (56)	71 (113)
1	Horiz. Displayed	28 (40)	50 (80)	28 (40)	50 (80)
2	Horiz. Sync. Pos	2D (45)	5A (90)	2D (45)	5A (90)
3	Horiz. Sync. Width	08 (8)	0E (14)	08 (8)	0E (14)
4	Vertical Total-1	1C (28)	1C (28)	7F (127)	3F (63)
5	Vert. Total Adjust	01 (1)	01 (1)	06 (6)	06 (6)
6	Vertic. Displayed	19 (25)	19 (25)	64 (100)	32 (50)
7	Vert. Sync Pos.	1A (26)	1A (26)	70 (112)	38 (56)
8	Interlace Mode	02 (2)	02 (2)	02 (2)	02 (2)
9	MaxScanLineAdd -1	08 (8)	08 (8)	01 (1)	03 (3)
10	Cursor Start	06 (6)	06 (6)	06 (6)	06 (6)
11	Cursor End	07 (7)	07 (7)	07 (7)	07 (7)
12	StartAddresss High	00 (0)	00 (0)	00 (0)	00 (0)
13	StartAddress Low	00 (0)	00 (0)	00 (0)	00 (0)

MODE SELECTION SUMMARY

MODE	'H3D8 BIT 0 HRESCK	'H3D8 BIT 4 HRESAD	'H3DE REG3 BIT 3 C4COLHR	'H3DE REG3 BIT 4 C16COL	'H3DE REG3 BIT 5 NVDM	'H3D8 BIT 1 GRPH	'H3DD BIT 0 EXTADR	'H3DF BIT 7 ADRM1	'H3DF BIT 6 ADRM0
40X25 ALPHA	0	0	0	0	0	0	0	0	0
80X25 ALPHA	1	0	0	0	0	0	0	0	0
160X200 16 COL	0	0	0	1	0	1	0	0	1
320X200 4 COL	0	0	0	0	0	1	0	0	1
320X200 16 COL	1	0	0	1	0	1	0	1	1
640X200 2 COL	0	1	0	0	0	1	0	0	1
640X200 4 COL	1	1	1	0	0	1	0	1	1

VIDEO/SYSTEM MEMORY ADDRESS MAP

'H0A0 BITS 4 3 2 1	VIDEO/SYSTEM MEMORY START ADDRESS	VIDEO/SYSTEM MEMORY LENGTH	VIDEO/SYSTEM MEMORY ADDRESS RANGE
0 0 0 0	0 0 0 0 0	128K	0 0 0 0 0 - 1 F F F F
0 0 0 1	2 0 0 0 0	128K	2 0 0 0 0 - 3 F F F F
0 0 1 0	4 0 0 0 0	128K	4 0 0 0 0 - 5 F F F F
0 0 1 1	6 0 0 0 0	128K	6 0 0 0 0 - 7 F F F F
0 1 0 0	8 0 0 0 0	128K	8 0 0 0 0 - 9 F F F F
1 0 0 1	0 0 0 0 0	256K	0 0 0 0 0 - 3 F F F F
1 0 1 0	2 0 0 0 0	256K	2 0 0 0 0 - 5 F F F F
1 0 1 1	4 0 0 0 0	256K	4 0 0 0 0 - 7 F F F F
1 1 0 0	6 0 0 0 0	256K	6 0 0 0 0 - 9 F F F F

VIDEO MEMORY ADDRESSING MODES

'H3DD BIT 0 EXTADR	'H3DF BIT 7 ADRM1	'H3DF BIT 6 ADRM0	VIDEO MEMORY ORGANIZATION (128)
0	0	0	1 16K Segment of Memory (8 Pages)
0	0	1	2 8K Segments of Memory (8 Pages) Switched on RA[0]
0	1	0	2 16K Segments of Memory (4 Pages) Switched on RA[0]
0	1	1	4 8K Segments of Memory (4 Pages) Switched on RA[0],RA[1]
1	0	0	1 32K Segment of Memory (4 Pages)
1	0	1	2 32K Segments of Memory (2 Pages) Switched on RA[0]

For 8 Page Modes CRTPG[2:0] select the Video Page
For 4 Page Modes CRTPG[2:1] select the Video Page
For 2 Page Modes CRTPG[2] select the Video Page

OTHER CHIP FUNCTIONS

In addition to the video controller functions, the Tandy 1000 video controller chip also provides most of the system address decode functions. These decode and chip select functions are described as follows:
A, B, C outputs are encoded device select lines and are connected to an external LS138.

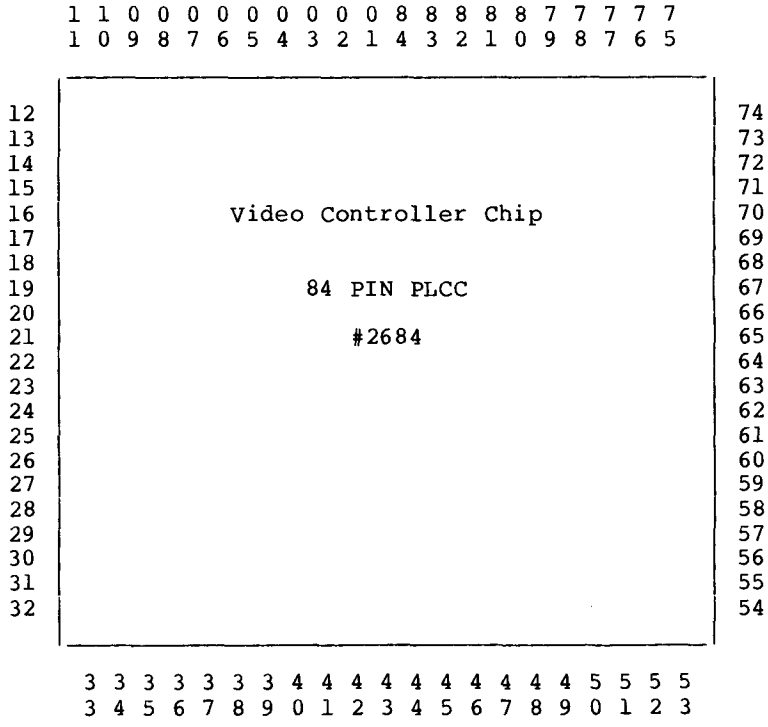
C	B	A	IOMB	BA0-15(HEX)	DESCRIPTION
1	1	1		NONE OF BELOW	
1	1	0	1	0020-0027	INTCSB
1	0	1	1	0040-0047	TMRCSB
1	0	0	1	0060-0067	PIOCSB
0	1	1	1	0200-0207	JOYSTKCSB
0	1	0	1	00C0-00C7	SNDCSB
0	0	1	1	03F0-03F7	FDCCSB
0	0	0	1	0378-037F	PRINTCSB

The output signal ROMIOSELB is the enable signal for an LS245 that controls all of the data flow to devices on the main logic board. This signal is active low and will be activated for any of the following conditions:

1. Video/System Memory Read or Write
2. Video Access at B8000-BFFFF
3. Rom Access at F0000-FFFFF
4. Video I/O access at 03D0-03DF
5. I/O access to any of the following addresses:

   0040-0047
   0060-0067
   00A0-00A7
   00C0-00C7
   0200-0207
   0378-037F
   03F0-03F7

PIN LIST


1 1 0 0 0 0 0 0 0 0 0 8 8 8 8 8 7 7 7 7 7
1 0 9 8 7 6 5 4 3 2 1 4 3 2 1 0 9 8 7 6 5
12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32
74 73 72 71 70 69 68 67 66 65 64 63 62 61 60 59 58 57 56 55 54
Video Controller Chip
84 PIN PLCC
#2684
3 3 3 3 3 3 3 4 4 4 4 4 4 4 4 4 5 5 5 5
3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3

DESCRIPTION OF EACH PIN FUNCTION

PIN#	PIN NAME	TYPE	DESCRIPTION
1	VSS	Ground	Ground
2	XMD[2]	Input/Output	External Memory Data I/O Bank 0
3	XMD[3]	Input/Output	External Memory Data I/O Bank 0
4	XMD[4]	Input/Output	External Memory Data I/O Bank 0
5	XMD[5]	Input/Output	External Memory Data I/O Bank 0
6	XMD[6]	Input/Output	External Memory Data I/O Bank 0
7	XMD[7]	Input/Output	External Memory Data I/O Bank 0
8	YMD[0]	Input/Output	External Memory Data I/O Bank 1
9	YMD[1]	Input/Output	External Memory Data I/O Bank 1
10	YMD[2]	Input/Output	External Memory Data I/O Bank 1
11	YMD[3]	Input/Output	External Memory Data I/O Bank 1
12	YMD[4]	Input/Output	External Memory Data I/O Bank 1
13	YMD[5]	Input/Output	External Memory Data I/O Bank 1
14	YMD[6]	Input/Output	External Memory Data I/O Bank 1
15	YMD[7]	Input/Output	External Memory Data I/O Bank 1
16	RFSHB	Input	Memory Refresh Strobe Input
17	MWE1B	Output	Ram Bank 1 Write Enable Signal
18	MWE0B	Output	Ram Bank 0 Write Enable Signal
19	RASB	Output	Ram Row Address Strobe
20	CASB	Output	Ram Column Address Strobe
21	BMEMRB	Input	CPU Memory Read Strobe
22	VDD	Power	5 Volts Supply
23	BMEMWB	Input	CPU Memory Write Strobe
24	CK28M	Clock	28.63636 Mhz Clock Input
25	VIDEOWAIT	Output(OpenDrain)	Video Wait Signal
26	SYSRSTB	Input	System Reset
27	IOMB	Input	CPU I/O-Memory Signal (Memory ->1, I/O -> 0)
28	A	Output	Encoded Peripheral Select Line
29	B	Output	Encoded Peripheral Select Line
30	C	Output	Encoded Peripheral Select Line
31	IOMEMSELB	Output	External Buffer Enable
32	NMIEN	Output	Nonmaskable Interrupt Enable
33	BIORB	Input	CPU I/O Read Strobe
34	BIOWB	Input	CPU I/O Write Strobe
35	LPIN	Input	Light Pen Signal Input
36	LPSWB	Input	Light Pen Switch Input
37	OUTVSYNC	Output	Vertical Sync Output
38	OUTHSYNC	Output	Horizontal Sync Output
39	COMPCOLOR	Output	Composite Color Signal
40	COMPSYNC	Output	Composite Sync Signal
41	OUTI	Output	Intensity Out
42	OUTR	Output	Red Video Out
43	VSS1	Ground	Ground
44	OUTB	Output	Blue Video Out/Monochrome Dotclock

45	OUTG	Output	Green Video Out/Monochrome Video
46	BA[19]	Input	CPU Address Line
47	BA[18]	Input	CPU Address Line
48	BA[17]	Input	CPU Address Line
49	BA[16]	Input	CPU Address Line
50	BA[157	Input	CPU Address Line
51	BA[14]	Input	CPU Address Line
52	BA[13]	Input	CPU Address Line
53	BA[12]	Input	CPU Address Line
54	BA[11]	Input	CPU Address Line
55	BA[10]	Input	CPU Address Line
56	BA[9]	Input	CPU Address Line
57	BA[8]	Input	CPU Address Line
58	BA[7]	Input	CPU Address Line
59	BA[6]	Input	CPU Address Line
60	BA[5]	Input	CPU Address Line
61	BA[4]	Input	CPU Address Line
62	BA[3]	Input	CPU Address Line
63	BA[2]	Input	CPU Address Line
64	BA[1]	Input	CPU Address Line
65	BA[0]	Input	CPU Address Line
66	DB[7]	Input/Output	CPU Data I/O
67	DB[6]	Input/Output	CPU Data I/O
68	DB[5]	Input/Output	CPU Data I/O
69	DB[4]	Input/Output	CPU Data I/O
70	DB[3]	Input/Output	CPU Data I/O
71	DB[2]	Input/Output	CPU Data I/O
72	DB[1]	Input/Output	CPU Data I/O
73	DB[0]	Input/Output	CPU Data I/O
74	MA[0]	Output	Memory Address Line
75	MA[1]	Output	Memory Address Line
76	MA[2]	Output	Memory Address Line
77	MA[3]	Output	Memory Address Line
78	MA[4]	Output	Memory Address Line
79	MA[5]	Output	Memory Address Line
80	MA[6]	Output	Memory Address Line
81	MA[7]	Output	Memory Address Line
82	BANKSL	Output	Memory Address Line
83	XMD[0]	Input/Output	External Memory Data I/O Bank 0
84	XMD[1]	Input/Output	External Memory Data I/O Bank 0

LOGIC BLOCK DIAGRAM

TEST MODES AND THEIR OPERATIONS

There are four Test Modes that the chip can be placed into to make the part easily and efficiently testable. All these Test Modes use conditions that can never occur in a System environment, therefore avoiding accidental entry in Test Mode. All the test modes are entered when both MEMRB and MEMWB are active. The selection of the different tests is done by an additional decode on some bits of the BA lines according to the following chart:

TEST MODE	ENABLED WHEN						OPERATION PERFORMED
	BMEMRB	BMEMWB	BA15	BA14	BA13	BA12	
1	0	0	1	X	X	X	Pinout the 6845 Megacell on external pins and/or Start Self Test Rom. While the testing of the Megacell is in progress, the Rom is performing a signature analysis. At the end of 4500 clocks, a PASS/FAIL bit is set, if the Self Test was successful.
2	0	0	0	1	X	X	Enable a Software Reset on the 6845.
3	0	0	0	X	1	X	Clear the Clock generators & blink counter to start from a known condition.
4	0	0	0	X	X	0/1	A 1 writes a bit that forces Display Enable constantly. A 0 removes forced Display Enable. Cleared by SYSRSTB.

TEST MODE 1 PINOUT THAT EMULATES THE 6845 STANDARD PRODUCT

The following signals of the Megacell are available on the following pins in Test Mode 1:

6845 SIGNAL	TAQUITA SIGNAL
RESETB	SYSRSTB
LPSTB	LPIN
MA[7:0]	MA[7:0]
MA[8]	BANKSL
MA[9]	MWE1B
MA[10]	ROMIOSELB
MA[11]	A
MA[12]	B
MA[13]	C
DE	COMPSYNC
CURSOR	COMPCOLOR
CLK	IOMB (See Note ***)
RNW	BIOWB
E	RFSHB
RS	BA[0]
CSB	LPSWB
DB[7:0]	DB[7:0]
RA[0]	RASB
RA[1]	CASB
RA[2]	OUTR
RA[3]	OUTI
RA[4]	MWE0B
HS	OUTHSYNC
VS	OUTVSYNC

Also the Pass/Fail bit for the Self Test Rom can be tested on the OUTG output pin during TEST MODE 1. Note that at least 4,500 clocks must be given in Test Mode 1 before checking the Pass/Fail bit. These clock times could be used to exercise the 6845 as a standard part according to the previous pinout.

Note*: IOMB is in fact CLK Bar so in order to test it using the standard part's test program, there is a need to invert the clock coming in the Test program.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAX RATINGS (NON-OPERATING, VSS=0v)

	MIN	MAX	UNITS
STORAGE TEMPERATURE	-65	150	DEGREES C.
VOLTAGE ON ANY PIN W.R.T.GROUND	-0.5	7.0	VOLTS

OPERATING ELECTRICAL SPECIFICATIONS

OPERATING AMBIENT AIR TEMP. RANGE	MIN	TYP	MAX	UNITS
	0	25	70	DEGREES C.

POWER SUPPLIES				
VCC SUPPLY VOLTAGE	4.5	5.0	5.5	VOLTS
VSS SUPPLY VOLTAGE	0	0	0	VOLTS
ICC SUPPLY CURRENT		20	35	MILLIAMPS
TOTAL POWER DISSIPATION (INCLUDE LOADING ON OUTPUTS)		100	175	MILLIWATTS

LEAKAGE CURRENT ALL INPUTS AND TRISTATE OUTPUTS	MIN	TYP	MAX	
	-10		10	MICROAMPS
INPUT VOLTAGES LOGIC "0" (Vil) ALL INPUTS			0.8	VOLTS
LOGIC "1" (Vih) ALL INPUTS	2.0			VOLTS

OUTPUT VOLTAGES	CURRENT LOADING	MIN	TYP	MAX	UNITS
LOGIC"0" (Vol) ALL OUTPUTS	2.0 MA			0.4	VOLTS
LOGIC"1" (Voh) ALL OUTPUTS	0.4 MA	2.4			VOLTS

INPUT CAPACITANCE	MIN	TYP	MAX	
ALL INPUTS			10	PICOFARADS

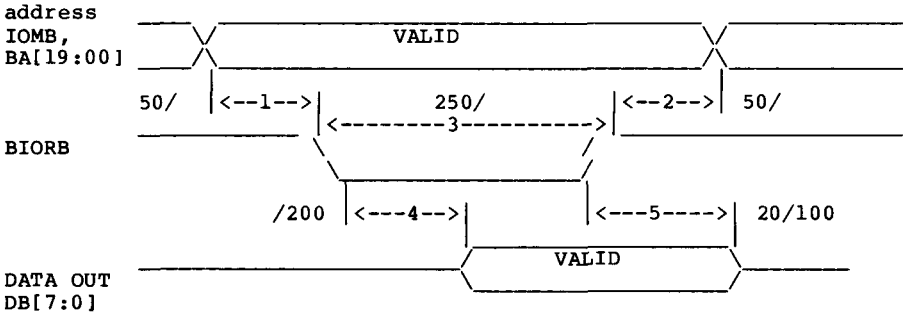
TIMING SPECIFICATION

MAXIMUM LOADING FOR EACH OUTPUT

MA[8]-MA[0]	100 pF
ALL OTHER OUTPUTS	20 pF

CHARACTERISTICS

READ Operation



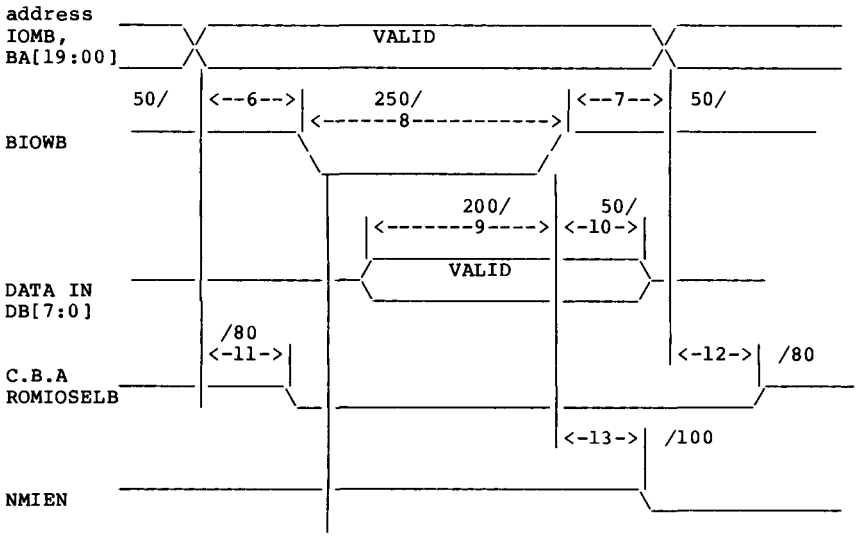
I/O TIMING

#	DESCRIPTION	MIN	MAX	UNITS	NOTE
1	ADDRESS VALID TO BIORB ACTIVE SETUP	50		NS	
2	ADDRESS VALID HOLD AFTER BIORB INACTIVE	50		NS	
3	BIORB PULSE WIDTH LOW	250		NS	
4	BIORB ACTIVE TO DATA OUT VALID		200	NS	
5	BIORB INACTIVE TO DATA OUT TRISTATE	20	100	NS	

READ OPERATION

READ OPERATION

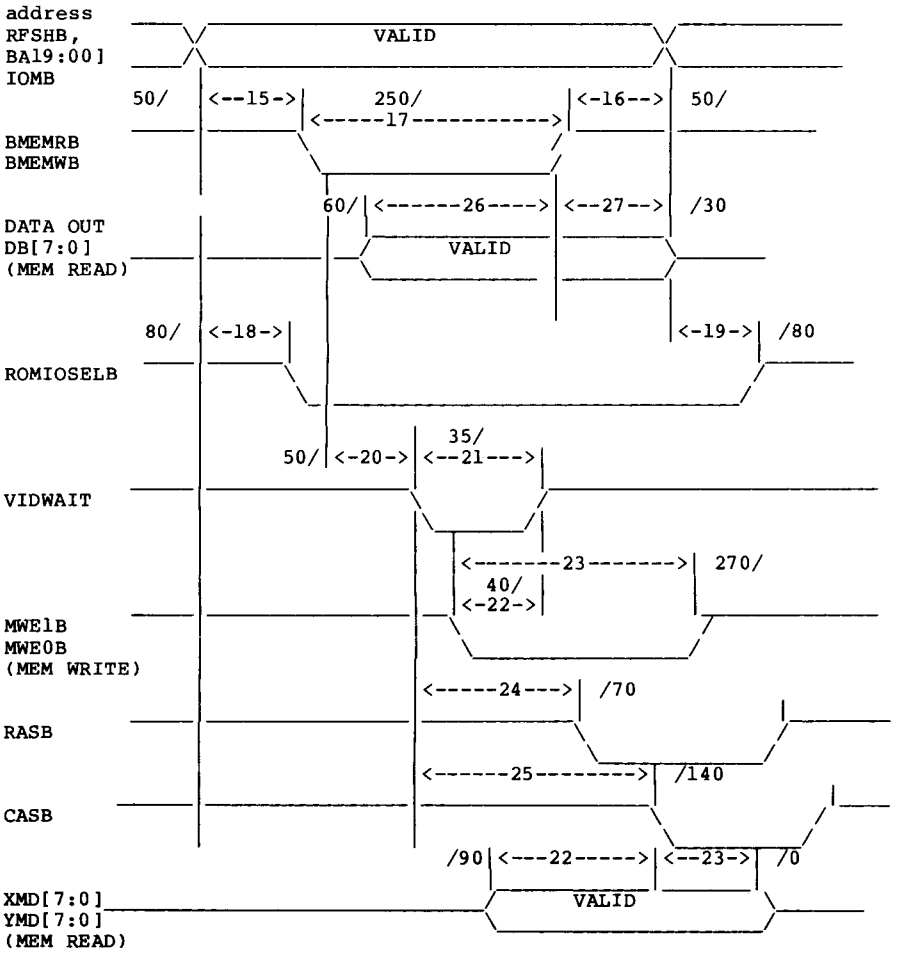
WRITE OPERATION AND I/O OUTPUT TIMING



#	DESCRIPTION	MIN	MAX	UNITS	NOTE
6	ADDRESS VALID TO BIOWB ACTIVE SETUP	50		NS	
7	ADDRESS VALID HOLD AFTER BIOWB INACTIVE	50		NS	
8	BIOWB PULSE WIDTH LOW	250		NS	
9	DATA IN VALID TO BIOWB INACTIVE SETUP	200		NS	
10	BIOWB INACTIVE TO DATA IN VALID HOLD	50		NS	
11	ADDRESS VALID TO C,B,A,ROMIOSELB OUTPUT DELAY		80	NS	
12	ADDRESS NOT VALID TO ROMIOSELB INACTIVE OUT DELAY	80		NS	
13	BIOWB INACTIVE TO NMIEN LATCHED OUTPUT DELAY		100	NS	

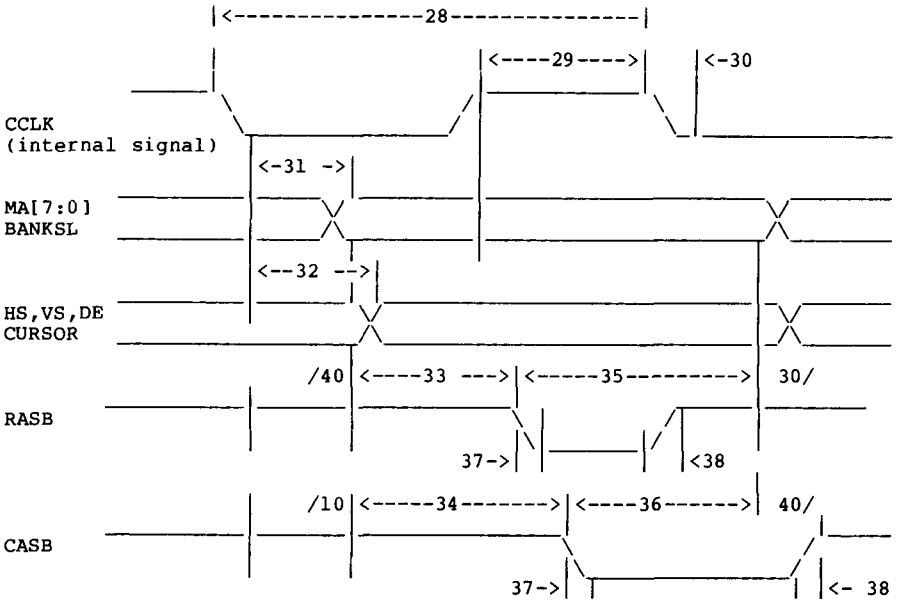
MEMORY DECODE TIMING

MEMORY READ OR WRITE OPERATION



*	DESCRIPTION	MIN	MAX	UNITS	NOTE
15	ADDRESS VALID TO BMEMRB ACTIVE SETUP	50		NS	
16	ADDRESS VALID HOLD AFTER BMEMRB INACTIVE	50		NS	
17	BMEMRB PULSE WIDTH LOW	250		NS	
18	ADDRESS VALID TO ROMIOSELB OUTPUT DELAY		80	NS	
19	ADDRESS NOT VALID TO ROMIOSELB INACTIVE OUT DELAY		80	NS	
20	VIDWAIT DELAY FROM BMEMRB READ LOW		50	NS	
21	VIDWAIT PULSE WIDTH	35	600	NS	
22	XMD, YMD SETUP TO CASB LOW (MEM READ)	90		NS	
23	XMD, YMD HOLD TO CASB LOW (MEM READ)	0		NS	
24	VIDWAIT LOW DELAY TO RASB LOW		70	NS	
25	VIDWAIT LOW DELAY TO CASB LOW	0	140	NS	
26	I/O DATA BUS OUT SETUP TO BMEMRB HIGH	60		NS	
27	I/O DATA BUS OUT HOLD TO BMEMRB HIGH	0	30	NS	

CRTC TIMING


28
29
30
CCLK
(internal signal)
31
MA[7:0]
BANKSL
32
HS,VS,DE
CURSOR
/40
33
35
30/
RASB
37
38
/10
34
36
40/
CASB
37
38

CRTC TIMING

	Characteristics	Symbol	Min	Nom	Max	Units
28	CCLK frequency	Fcyc			2	MHz
29	CCLK width	PWcl	100			nS
30	CCLK rise and fall time	Tcr,Tcf			5	nS
31	CLK fall to MA[7:0]RA0-4 delay time	Tmad,Trad			50	nS
32	CLK fall to HS, VS, DE,CURSOR delay time	Thsd,Tvsd Tdtd,Tcdd			50	nS
33	MA[7:0],BANKSL setup to RASB low		40			nS
34	MA[7:0],BANKSL setup to CASB low		10			nS
35	MA[7:0],BANKSL hold from RASB low		30			nS
36	MA[7:0],BANKSL hold from CASB low		40			nS
37	RASB,CASB fall				20	nS
38	RASB,CASB rise				5	nS

OTHER TIMING SPECS

	Characteristics	Symbol	Min	Nom	Max	Units
39	Relative Skew of R,G,B,I				10	nS
40	Relative Skew of R,G,B,I With respect to Compcol				20	nS
41	Relative Skew of R,G,B,I With respect to CompSync OutHsync,OutVsync				35	nS
42	Relative Skew of R,G,B,I With respect to CompSync				35	nS

MEGACELL 6845R1 SPECIFICATION DATASHEET FOR 6845 MEGACELL

VE 68C45 MEGACELL DESIGN KIT
CRT CONTROLLER MEGACELL

FEATURES

- Completely integrated with VTI's extensive IC design tools and libraries
- CMOS (2-micron) M68C45 Megacell configurable as:
  - -- 68C45R - CMOS equivalent of Motorola 6845R CRTC
  - -- 68C45R1 - CMOS equivalent of Motorola 6845R1 Enhanced CRTC
  - -- 68C45S - CMOS equivalent of Hitachi 6845S CRTC
  - -- 68C45SY - CMOS CRTC similar to Synertek 6545 CRTC
- 4.5 MHz video memory interface
- 3 MHz system processor interface
- Compatible with the VTI bus architecture
- Programmable Display Enable and Cursor delays (standard for S and SY versions -- optional for R and R1 versions)
- Programmable Vertical Sync pulse width (standard for S version -- optional for R, R1 and SY versions)
- Row/Column display memory addressing (SY version)
- Double Width character control

OPTIONAL FEATURES

- 16K, 32K, or 64K display Memory Address range (14, 15, or 16 bits)
- 7, 8, or 9-bit Vertical Row counter

VTI MEGACELLS

Megacells are building block equivalents of standard LSI functions that can be combined with other megacells, standard cells or compiled cells to create custom User-Specific ICs (USICs). Megacells are fully compatible with VTI's other cell technologies and design tools.

The VTI bus (TM) architecture allows multiple megacells to be combined on a single IC, along with additional cells from VTI's extensive libraries -- decreasing the design time, design cost, and size of complex systems. A detailed Functional Model provided with each megacell further reduces design verification time.

SIGNAL DESCRIPTIONS

The following signals function the same on the M68C45 Megacells and on the standard VL6845 family of CRT Controller ICs.

Signal	I/O	Description
RS	IP	Register Select
E	IP	Enable
RNW	IP	Specify READ (high) or WRITE (low) operation
CSB	IP	Chip (6845 megacell) select, low true
CCLK	IP	Character Clock
LPSTB	IP	Light Pen Strobe
D0-D7	I/O	Data Bus
RA0-RA4	OP	Raster Address
HS	OP	Horizontal Sync
RESETB	IP	Reset, low true

The following signals are unique to the VE68C45 Megacells, or are functionally different on the VE68C45 Megacells and the VL6845 ICs.

Signal	I/O	Description
DE	OP	Display Enable output - active (DE = "1") when the VE68C45 is generating active display information. The S version can be programmed with a 0, 1, or 2 character delay. The SY version can be programmed for a 0 or 1 character delay.
CURSOR	OP	Cursor output - this signal is high when the raster scan coincides with the programmed cursor position. The S version can be programmed with a 0, 1, or 2 character delay. The SY version can be programmed for a 0 or 1 character delay.
VS	OP	Vertical Sync output - active high pulse which determines the vertical placement of the video data. An optional feature permits programming the Vertical Sync pulse width.

MA0-MA13, 14,15	OP	14, 15, or 16- bit Video Memory Address bus. These tri-state outputs provide the binary address to the external video RAM. If row/column addressing is selected (SY version only) this bus will provide row/column addressing to the external RAM instead of binary addressing. The AENB input signal can be used to place the MA bus in the high impedance state.
AENB	IP	Address Enable input - when asserted low (AENB = "0") the MA outputs are enabled. AENB = "1" forces the MA outputs into a high impedance state.
LD0-LD13, 14,15	I/O	14, 15, or 16-bit Advanced Memory Address bus - separate video memory address information on this bus precedes the information on the MA bus by one character clock. This bus is provided to interface with a separate strip of logic for split display capability.
LOAD	IP	When asserted (high) a new value is loaded into the RA counter. Tie to VSS when not used.
BREAK	IP	To be used for splitted screen format. Tie to VSS when not used.
READB	OP	This signal goes LOW during a legitimate read operation.
VDRA (reserved)	n/c	Reserved for future expansion. To be left unconnected.
DW	IP	Double Width input - this input puts the VE68C45 in a double-width display mode. Tie to VSS when not used.

6845R, 6845S, 6545SY	IP	One of these three inputs is tied high to select the version of the VE68C45 used in your application. The remaining two inputs must be grounded. NOTE: the VE68C45SY does not provide 6545 transparent addressing or the 6545 status register.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Ambient temperature under bias	0 C to 70 C
Storage temperature	-65 C to +150 C
Voltage on any signal with respect to Gnd	-0.5V to +7V
Power dissipation	750mW

DC characteristics (Ta = 0 - 70 degree C, Vss=0v, Vcc=+5 +/- 10%)

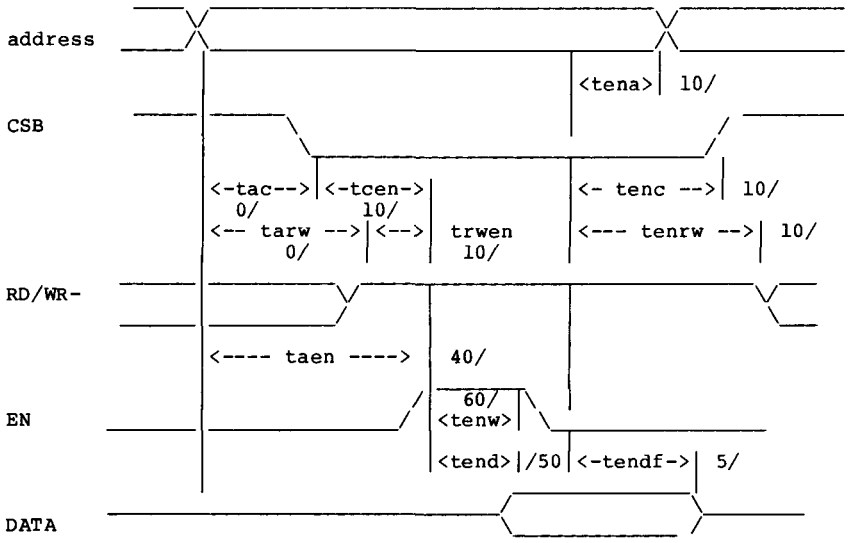
Characteristics	Symbol	Min	Typ	Max	Units
Input High Voltage					
Inputs,I/O	Vih	3.0		Vcc	Volts
Input Low Voltage					
Inputs,I/O	Vil	Vss		0.8	Volts
Output High Voltage					
Outputs,I/O	Voh	3.0		Vcc	Volts
Output Low Voltage					
Outputs,I/O	Vol			0.4	Volts

Capacitance

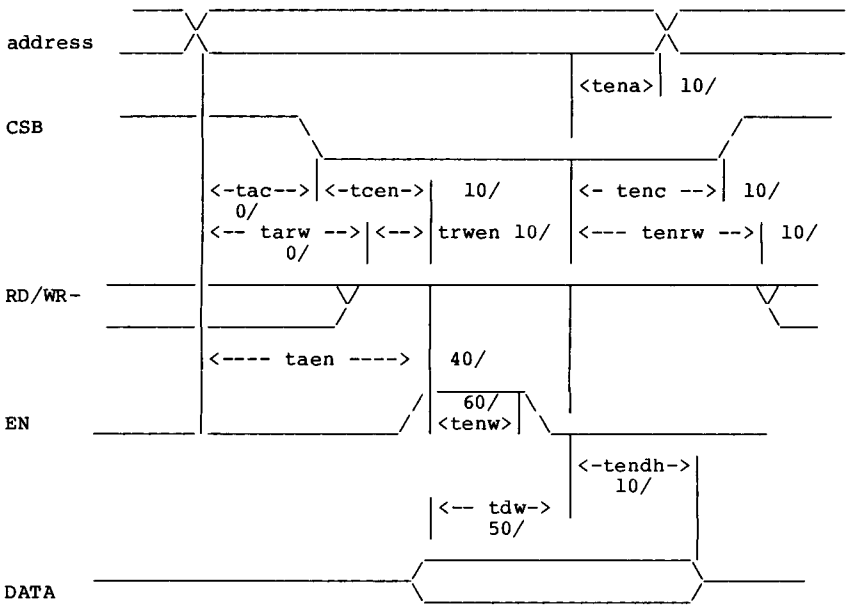
Input Capacitance					
CLK input	Cin			6	pF
remaining inputs	Cin			.7	pF
Output Loading					
MA0-13,D0-7	Cout			9	pF
RA0-4,HS,VS,DE, Cursor	Cout			3	pF

AC CHARACTERISTICS (Vcc=+5v +/- 10%, Vss=0v, Ta=0 C to 70 C)

VTI BUS TIMING



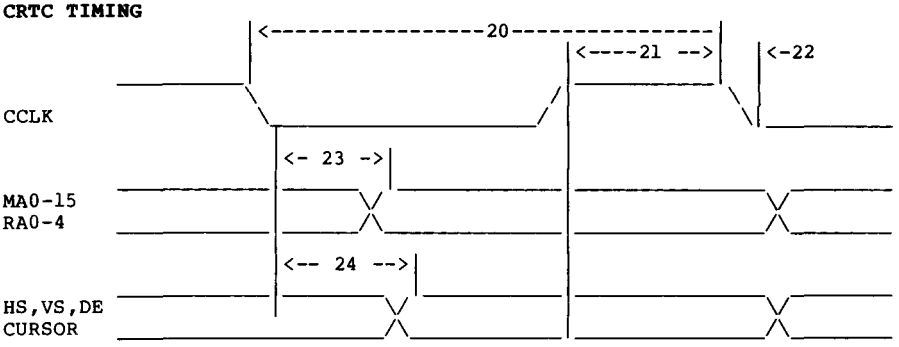
WRITE


address
CSB
RD/WR-
EN
DATA
<tena> 10/
<-tac--> 0/
<-tcen-> 10/
<- tenc --> 10/
<-- tarw --> 0/
<--> trwen 10/
<--- tenrw --> 10/
<---- taen ----> 40/
60/
<tenw>
<-tendh-> 10/
<-- tdw-> 50/

VTI BUS TIMING

	MIN(ns)	MAX(ns)
TAC address to CS delay	0	
TARW address to read/write delay	0	
TAEN address to enable set up	40	
TCEN CS to enable delay	10	
TRWEN read/write to enable set up	10	
TENW enable pulse width	100	
TENA enable to address hold time	10	
TENC enable to cs hold time	10	
TENRW enable to read/write hold time	10	
read:		
TEND enable to read data delay		50
TENDF enable to data bus float	5	30
write:		
TDEN write data to enable setup time	50	
TENDH enable to write data hold time	10	

CRTC TIMING



CRTC TIMING

	Characteristics	Symbol	Min	Nom	Max	Units
20	CLK frequency	Fcyc			4.5	MHz
21	CLK width	PWcl	100			nS
22	CLK rise and fall time	Tcr,Tcf			5	nS
23	CLK fall to MA0-15,RA0-4 delay time	Tmad,Trad			50	nS
24	CLK fall to HS, VS, DE,CURSOR delay time	Thsd,Tvsd Tdtd,Tcdd			50	nS

DMA CHIP SPECIFICATION

DMA CHIP SPECIFICATION
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PIN LIST.....5
PIN FUNCTIONS.....6
LOGIC BLOCK DIAGRAM.....10
ELECTRICAL SPECIFICATIONS.....11
TIMING.....18

DMA CHIP SPECIFICATION

GENERAL DESCRIPTION

The DMA Chip is an Intel 8237A-5 (AMD 9517) DMA Controller plus associated support circuity to integrate the TANDY 1000 External Memory function into a single ASIC part. The support circuity is divided into the five functional sections. The ADDRESS DECODE-MEMORY and ADDRESS DECODE-IO are independent of the DMA function and interface directly into the bus. The TIMING and DMA RDY sections are DMA support functions. The BUFFERS support the in/out pins.

The functional configuration of the 8237 for the DMA Chip is a fixed subset of its total capability. It is configured via the BIOS ROM for: normal timing, fixed priority, late write, high DREQ sense, low DACK sense.

ADDRESS DECODE - MEMORY

Provides RAM Memory access decode and address generation. Bus addresses A19-A15 determine which segment(bank) of memory is being accessed based on one of four possible memory configurations. (see memory map Figure 1). This is combined with Bus strobes MEMWB or MEMRB and CLK to create one of the three RAS strobes (RAS0B, RAS1B or RAS2B), MUX, CAS, data directional controls DBDIR, DBENB and the multiplexed RAM addresses MA0-MA8. The signals CAS and MUX will occur for all access's except REFRESH. The address lines MA0-MA8 are Bus addresses A0-A8 and A9-A17 multiplexed together by the signal MUX. These will occur for all access's including REFRESH (since MUX does not occur during REFRESH, MA0-MA8 will be only A0-A8). The selection of MA8 will be made externally since Bank 0 and Bank 1 can be either 64K or 265K DRAM IC's.

	MCF0,MCF1 CODE	MEMORY ORGANIZATION	ADDRESS	ACCESS CONTROL SIGNAL
OPTION #1	00	BANK 0 64K x 8	0.0000-0.FFFF	RAS0
		BANK 1 64K x 8	1.0000-1.FFFF	RAS1
		BANK 2 EMPTY		
OPTION #2	01	BANK 0 256K x 8	0.0000-3.FFFF	RAS0
		BANK 1 EMPTY		
		BANK 2 EMPTY		
OPTION #3	10	BANK 0 256K x 8	0.0000-3.FFFF	RAS0
		BANK 1 256K x 8	4.0000-7.FFFF	RAS1
		BANK 2 EMPTY		
OPTION #4	11	BANK 0 64K x 8	0.0000-0.FFFF	RAS0
		BANK 1 64K x 8	1.0000-1.FFFF	RAS1
		BANK 2 256K x 8	2.0000-5.FFFF	RAS2

Figure 1 MEMORY CONFIGURATION MAP

EQUATIONS FOR RAS-B

64K DRAMS require address A0-A15, therefore A19-A16 determine access.
256K DRAMS require address A0-A17, therefore A19-A18 determine access.

```
RAS0B = /MCF1./MCF0./19./18./17./16./REFRESH.(MEMRB+MEMWB)  OPTION #1
      + /MCF1. MCF0./19./18.        /REFRESH.(MEMRB+MEMWB)  OPTION #2
      +  MCF1./MCF0./19./18.        /REFRESH.(MEMRB+MEMWB)  OPTION #3
      +  MCF1. MCF0./19./18./17./16./REFRESH.(MEMRB+MEMWB)  OPTION #4
      +  REFRESH.MEMRB

RAS1B = /MCF1./MCF0./19./18./17. 16./REFRESH.(MEMRB+MEMWB)  OPTION #1
      +  MCF1./MCF0./19. 18.        /REFRESH.(MEMRB+MEMWB)  OPTION #3,
                                                        NO OPTION #2
      +  MCF1. MCF0./19./18./17. 16./REFRESH.(MEMRB+MEMWB)  OPTION #4
      +  REFRESH.MEMRB

RAS3B =  MCF1. MCF0./19./18. 17     /REFRESH.(MEMRB+MEMWB)  OPTION #4,
                                              NO OPTION #1,#2,#3
      +  MCF1. MCF0./19. 18./17     /REFRESH.(MEMRB+MEMWB)
      +  REFRESH.MEMRB
```

EQUATIONS FOR MULTIPLEXED ADDRESSES MA-

	ROW ADDRESS (FIRST)	COLUMN ADDRESS (SECOND)	
MA0 :	A0	A8	Since these addresses will
MA1 :	A1	A9	be used for either/both
MA2 :	A2	A10	64K and 256K DRAMS, MA8
MA3 :	A3	A11	will be A16,A17 instead
MA4 :	A4	A12	of two sets of MAs.
MA5 :	A5	A13	(i.e. 64K MA0=A0/A8,
MA6 :	A6	A14	256K MA0=A0/A9,...etc.)
MA7 :	A7	A15	
MA8 :	A16	A17	

ADDRESS DECODE - I/O

Provides I/O decode for generating the chip selects for the DMA Controller and the DMA Segment Address Register plus the data directional control signals DBDIR and DBENB. Bus addresses A0-A15 are decoded and combined with Bus strobes IORB or IOWB to create the chip selects.

CHIP SELECT FUNCTION	ADDRESS	SIGNAL	EQUATION (A19-A16 = don't care) (A15,...,A8 = 0, ALWAYS)
DMA	X.0000-X.000F	DMACSB =	/A7./A6./A5./A4./AEN.(IORB + IOWB)
DMA SEGMENT REGISTER	X.0080-X.0083	WPRCSB =	A7./A6./A5./A4./A4./AEN.IOWB

Figure 2 I/O CONFIGURATION MAP

DMA READY

A system requirement is to have one WAIT cycle automatically inserted into each I/O transfer. When an IORB occurs, WAIT cycles will continually be inserted until IORB returns inactive or until a MEMWB or MEMRB occurs.

This one WAIT cycle is inserted automatically when the CPU is Bus Master. Therefore when the DMA is a Bus Master, it is necessary to insert one WAIT cycle into each DMA I.O transfer (that is every transfer) and honor any additional WAIT requests from the system.

TIMING GENERATOR

The input clock is OSC (= 14.31818 MHZ).

1.) It is divided by three to recreate the 4.77 MHz system processor clock which is used as the clock for the 8237.

2.) It is used to delay the memory access strobe MEM-B twice to create the timing for RAS-, MUX, and CAS.

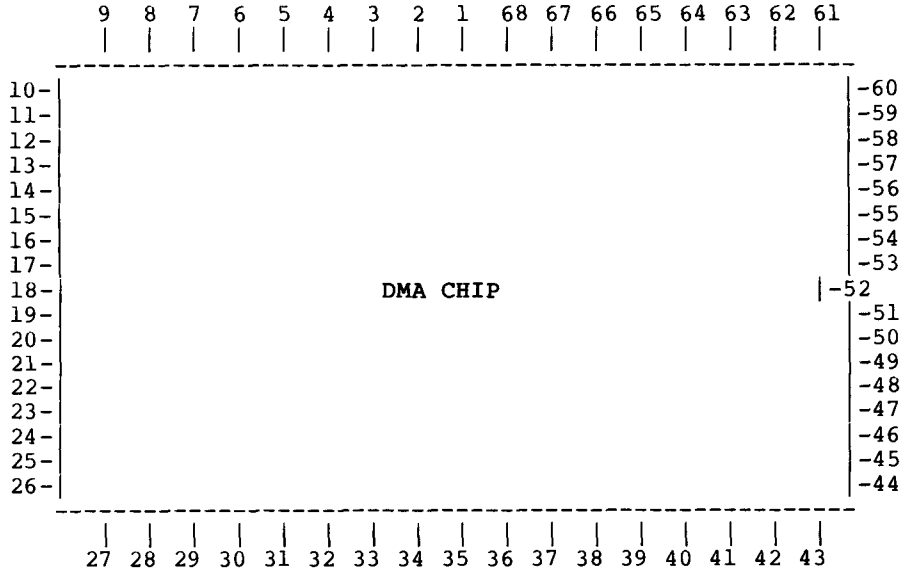
BUFFERS

Provide isolation and drive capability since this circuit will interface directly onto the system bus. These buffers include the bi-directional buffers for address and control strobes (CPU Bus Master - Receive control,address, DMA Bus Master - transmit control,address) but excludes the bi-directional data buffer. Since it must be shared by the memory, this part will be provided externally. Decoding from the ADDRESS DECODE I/O and MEMORY circuitry are combined to provide directional control signals DBDIR, DBENB for this data bus buffer.

FUNCTION	SIGNAL	EQUATION
DATA BUS DIRECTIONAL CONTROL	DBDIR	= DMACSB.IORB + /MCF1./MCF0./19./18./17. /REFRESH. MEMRB + /MCF1. MCF0./19./18. /REFRESH. MEMRB + MCF1. /MCF0./19. /REFRESH. MEMRB + MCF1. MCF0./19.(/18 + 18./17)./REFRESH. MEMRB
DATA BUS BUFFER ENABLE	DBENB	= DMACSB + WPRCSB + /MCF1./MCF0./19./18./17. /REFRESH. MEM-B + /MCF1. MCF0./19./18. /REFRESH. MEM-B + MCF1. /MCF0./19. /REFRESH. MEM-B + MCF1. MCF0./19.(/18 + 18./17)./REFRESH. MEM-B
ADDRESS BUS, CONTROL BUS DIRECTIONAL CONTROL	DMAAENB	= 8257 Signal AEN inverted

Figure 3 BUFFER CONTROL SIGNALS

PIN LIST


9 8 7 6 5 4 3 2 1 68 67 66 65 64 63 62 61
10- -60
11- -59
12- -58
13- -57
14- -56
15- -55
16- -54
17- -53
18- DMA CHIP -52
19- -51
20- -50
21- -49
22- -48
23- -47
24- -46
25- -45
26- -44
27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43

DESCRIPTION OF EACH PIN FUNCTION

FUNCTION	PIN NUMBER	FUNCTION	PIN NUMBER
VSS	1	VDD	35
RFSHB	2	CASB	36
REFRESHB	3	RAS0B	37
MCF1	4	RAS1B	38
MCF0	5	RAS2B	39
WRB	6	MA0	40
FDCDMACKB	7	MA1	41
DACK1B	8	MA2	42
DACK3B	9	MA3	43
DMATC	10	MA4	44
FDCDMARQB	11	MA5	45
DRQ1B	12	MA6	46
DRQ3B	13	MA7	47
DBDIR	14	MA8	48
DBEN	15	A19	49
MEGAPIN	16	A18	50
OSC	17	A17	51
VSS2	18	A16	52
BREQB	19	A15	53
RESET	20	A14	54
AENA	21	A13	55
BRDY	22	A12	56
MEMWB	23	A11	57
MEMRB	24	A10	58
IOWB	25	A9	59
IORB	26	A8	60
D7	27	A7	61
D6	28	A6	62
D5	29	A5	63
D4	30	A4	64
D3	31	A3	65
D2	32	A2	66
D1	33	A1	67
D0	34	A0	68

PIN DEFINITIONS

NOTE: All negative true signals use the suffix "B".

INPUTS: (11 pins)

MCF0	Memory configuration OPTION Select.
MCF1	(See Figure 1 for details.)
RFSH	8237 CHANNEL 0 REQUEST (DREQ2) Input from timer. Set up as 16 microsec interval timer for REFRESH.
DRQ1	8237 CHANNEL 1 REQUEST (DREQ1)
FDCDMARQ	8237 CHANNEL 2 REQUEST (DREQ2) dedicated to FDC.
DRQ3	8237 CHANNEL 3 REQUEST (DREQ3)
READY	System READY signal for DMA.
RESET	System hardware master RESET.
OSC	Memory timing clock. Currently CLK14M.
AEN	CPU Bus Grant (8237 HLDA)
TEST	Input for TEST mode used by IC mfg.

BI-DIRECTIONAL: (32 pins)

BUSA19-BUSA16	System Segment Address (CPU BUS MASTER- INPUT, DMA BUS MASTER- OUTPUT)
BUSA15-BUSA0	System Address (CPU BUS MASTER- INPUT, DMA BUS MASTER- OUTPUT)
D00-D07	System Data Bus (WRITE-OUTPUT, READ- INPUT)
MRB	System Memory Read strobe (CPU BUS MASTER- INPUT, DMA BUS MASTER- OUTPUT)
MWB	System Memory Write strobe (CPU BUS MASTER- INPUT, DMA BUS MASTER- OUTPUT)
IRB	System Memory Read strobe (CPU BUS MASTER- INPUT, DMA BUS MASTER- OUTPUT)
IWB	System Memory Write strobe (CPU BUS MASTER- INPUT, DMA BUS MASTER- OUTPUT)

OUTPUTS: (20 pins)

MA00-MA08	External Memory multilplexed address
RAS0B-RAS2B	External Memory ROW strobes.
CASB	External Memory COLUMN strobe.
WRB	External Memory WRITE strobe.
DBDIR	Data Buffer directional control (Read=1).
DBENB	Data Buffer enable.
REFRESHB	8237 CHANNEL 0 ACKNOWLEDGE (DREQ0) Acknowledge from DMA channel 0 setup for refresh.
DACK1B	8237 CHANNEL 1 ACKNOWLEDGE (DREQ1)
FDCDMACKB	8237 CHANNEL 2 ACKNOWLEDGE (DREQ2)
DACK3B	8237 CHANNEL 3 ACKNOWLEDGE (DREQ3)
DMATC	8237 EOP (output only)
BREQB	CPU Bus Request (8237 HRQ)

POWER: (4 pins)

VDD	+5 VDC
VSS	GND

TOTAL PIN COUNT = 68

PIN SENSE	DMA PINOUT	8237 PINOUT
BIDIR	A0	A0
BIDIR	A1	A1
BIDIR	A2	A2
BIDIR	A3	A3
TSFBAK	A4	A4
TSFBAK	A5	A5
TSFBAK	A6	A6
TSFBAK	A7	A7
TSFBAK	A8	
TSFBAK	A9	
TSFBAK	A10	
TSFBAK	A11	
TSFBAK	A12	
TSFBAK	A13	
TSFBAK	A14	
TSFBAK	A15	
TSFBAK	A16	
TSFBAK	A17	
TSFBAK	A18	
TSFBAK	A19	

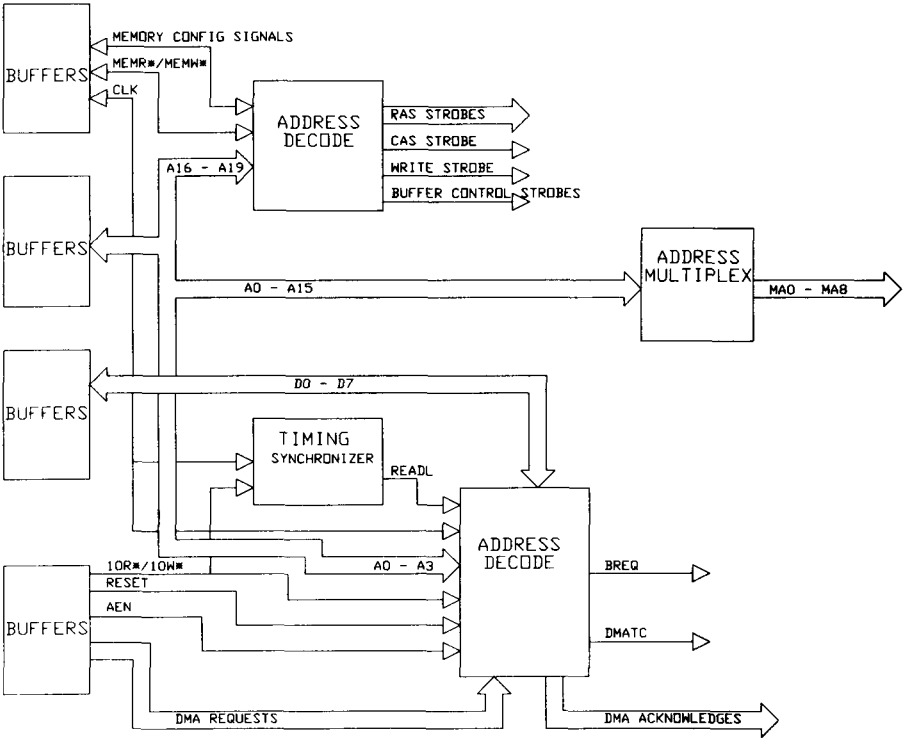
(BIDIR ENA = DMAAEN)

(BIDIR ENA =8237 CNTL)

(TS ENA = DMAAEN)

(TS ENA = LOGIC 1)

PIN SENSE	DMA PINOUT	8237 PINOUT
BIDIR	D0	D0
BIDIR	D1	D1
BIDIR	D2	D2
BIDIR	D3	D3
BIDIR	D4	D4
BIDIR	D5	D5
BIDIR	D6	D6
BIDIR	D7	D7
OUTPUT	MAD0	
OUTPUT	MAD1	
OUTPUT	MAD2	
OUTPUT	MAD3	
OUTPUT	MAD4	
OUTPUT	MAD5	
OUTPUT	MAD6	
OUTPUT	MAD7	
TRISTATE	MAD8	
INPUT	RESET	RESET
INPUT	READY	RDY (MUXED)
OUTPUT	DMATC	EOP* (INVERTED)
OUTPUT	BREQ*	HRQ (INVERTED)
INPUT	OSC	CLK (MUXED)
INPUT	DRQ3	DREQ3
INPUT	FDCDMARQ*	DREQ2
INPUT	DRQ1*	DREQ1
INPUT	RFSH*	DREQ0 (MUXED)
OUTPUT	REFRESH*	DACK0
OUTPUT	DACK1*	DACK1
OUTPUT	FDCDMACK*	DACK2
OUTPUT	DACK3*	DACK3
OUTPUT	RAS0	
OUTPUT	RAS1	
OUTPUT	RAS2	
OUTPUT	CAS	AS (MUXED)
OUTPUT	WR*	AEN (MUXED)
INPUT	MCF1	CS (MUXED)
INPUT	MCF0	
OUTPUT	DBDIR	
OUTPUT	DBEN	
INPUT	AEN (SYSTEM)	HLDA
BIDIR	MEMW* -	MW* -
BIDIR	MEMR* | (BIDIR ENA	MR* | (BIDIR ENA
BIDIR	IOW* | = DMAAEN)	IOW* |- =8237 CNTL)
BIDIR	IOR* -	IOR* -
POWER	VDD	VDD
POWER	VDD	VDD
GROUND	VSS	VSS
GROUND	VSS	
	68 PINS	40 PINS



LOGIC BLOCK DIAGRAM

ELECTRICAL SPECIFICATIONS - DMA

ELECTRICAL PARAMETERS

ABSOLUTE MAX RATINGS (NON-OPERATING, VSS=0.0V)

	MIN	MAX	UNITS
STORAGE TEMPERATURE	-65	+150	DEGREES C.
VOLTAGE ON ANY PIN W.R.T.GROUND	-0.5	7.0	VOLTS

OPERATING ELECTRICAL SPECIFICATIONS:

OPERATING AMBIENT	MIN	TYP	MAX	UNITS
AIR TEMP. RANGE	0	25	70	DEGREES C
POWER SUPPLIES				
VDD	4.5	5.0	5.5	VOLTS
VSS	0	0	0	VOLTS
ICC			100	MILLIAMPS

NOTE: INCLUDE ALL RELEVENT CONDITIONS UNDER WHICH ICC IS TO BE MEASURED; IE, ALL INPUTS AT VSS OR VCC, CLOCK FREQUENCY, ETC.

TOTAL POWER DISSIPATION (Include output loading)			700	MILLIWATTS

LEAKAGE CURRENT	MIN	TYP	MAX
Vin = 0.0 v		20	microamps
Vin = 5.0 v		-20	microamps

INPUT VOLTAGES

LOGIC "0" (Vil)		0.8	volts
LOGIC "1" (Vih)	2.0		volts

OUTPUT VOLTAGES	CURRENT LOADING	MIN	TYP	MAX	UNITS
LOGIC "0" (Vol) @ 4.0 MA LOAD				0.4	volts
LOGIC "1" (Voh) @ 0.4 MA LOAD		2.4			volts

INPUT CAPACITANCE		MIN	TYP	MAX
All inputs	0.0 < Vin < 5.0	10		picofarads

OUTPUT CAPACITANCE			
All outputs Except Data (bi-directional)	50		picofarads

BI-DIRECTIONAL CAPACITANCE

SEE NOTES 3-6 IN THE FOLLOWING SECTION.

TIMING SPECIFICATION

MAXIMUM LOADING FOR EACH OUTPUT

Capacitive Load:50pf
Current Load: Ioh = 4.0 MA
Iol = 0.4 MA

INPUT/OUTPUT TIMING

(NOTE: ALL AC TESTING AND TIMING MEASUREMENTS WILL BE AT THE FOLLOWING CONDITIONS: VOH (OUTPUT 1 LEVEL) = 2.0V, AND VOL (OUTPUT 0 LEVEL) = .8V)

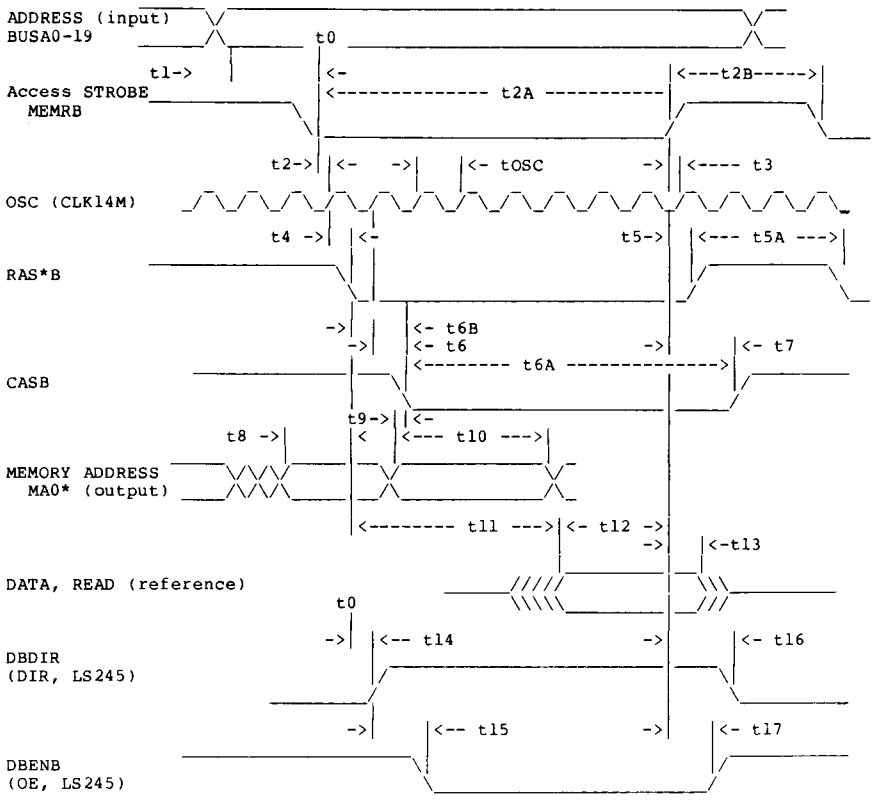


Figure 1. MEMORY TIMING PARAMETERS, READ

MEMORY TIMING PARAMETERS , READ

	min	typ	max	
t0 Reference time zero, STROBE lo tOSC Period of 14.31818 MHz		69.8		
t1 ADDRESS Setup to STROBE lo	50			
t2 STROBE lo Setup to OSC hi	15			
t2A STROBE lo Length		250		
t2B STROBE hi Length		250		
t3 STROBE hi Setup to OSC hi	don't care			
t4 RAS*B lo Delay from OSC hi	0		40	
t5 RAS*B hi Delay from STROBE hi	0		40	
t5A RAS*B hi Length	100			
t6 CAS*B lo Delay from OSC hi	0		40	
t6A CAS*B lo Length	75			
t6B CAS*B lo Delay from RAS*B lo		69.8	70	
t7 CAS*B hi Delay from STROBE hi		69.8	70	
t8 MA*-Row Address Valid Setup to RAS*B lo	20			NOTE 2
t9 MA*-Column Address Valid Setup to CAS*B lo	20			NOTE 2
t10 MA*-Column Address Hold	35			
t11 DATA Valid Delay from RAS*B True (reference)		150		NOTE 6
t12 DATA Valid Setup to STROBE hi	70			NOTE 3
t13 DATA Hold from STROBE False hi	0			
t14 DBDIR lo Delay from STROBE lo			40	
t15 DBENB lo Delay after DBDIR hi		70		NOTE 4
t16 DBENB Hold from STROBE hi	0			
t17 DBDIR Hold from DBENB hi	0			NOTE 5

NOTE 1 Setup time t2 will be defined by the ASIC design. It should be of sufficient length to allow Clear on RAS flip-flop to go false and still meet setup time before next clock rising edge.

NOTE 2 Address outputs are loaded with 3 row x 8 DRAMS = 24 x 8 pf = 192 pf. each.

NOTE 3 Additional delay through LS245 needs to be added to match Bus Specs.
Bus requires +75 ns setup. LS245 into 45pf requires 20 ns. Therefore 75+20=95 ns.

NOTE 4 Applying the DIRection signal to the LS245 and allowing the part to settle before applying OUTput ENable reduces Bus and power noise. Also OUTput ENable should be removed first.

NOTE 5 OUTput ENable should be removed first before changing DIRection.

NOTE 6 Depends upon DRAM used.

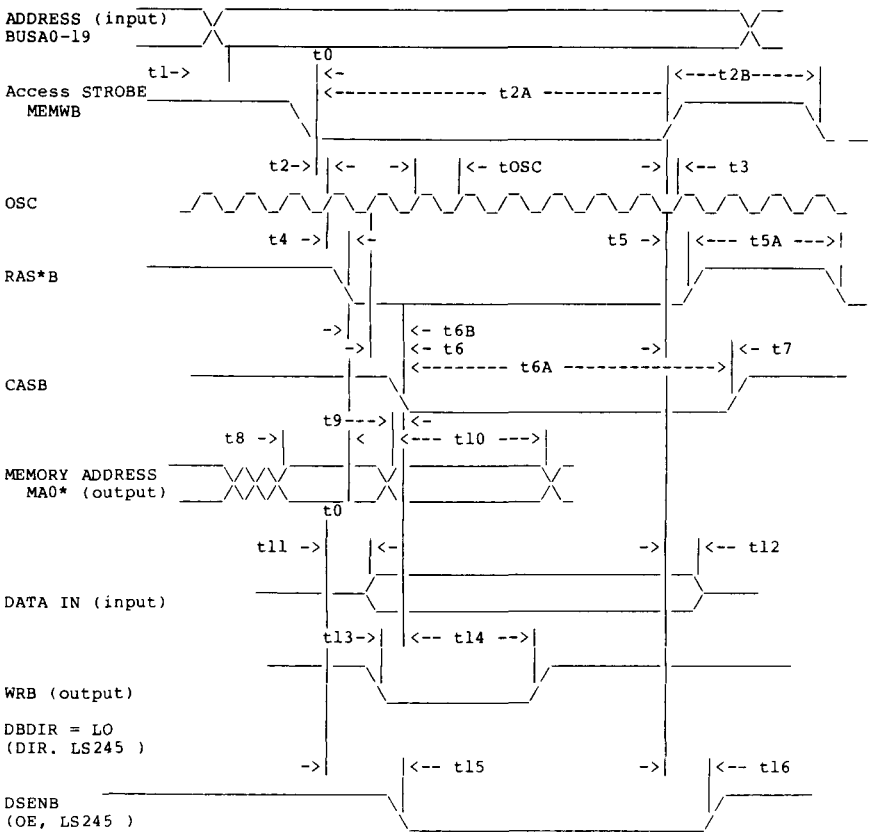


Figure 2. MEMORY TIMING PARAMETERS, WRITE

MEMORY TIMING PARAMETERS, WRITE

	min	typ	max	
t1 thru t10, see MEMORY TIMING PARAMETERS, READ				
t11 DATA Valid Delay after STROBE lo			50	NOTE 1 [1]
t12 DATA Valid Hold after STROBE hi	20			{2}
t13 WRB lo Setup to CASB lo	30			(3)
t14 WRB lo Hold after CASB lo	70			(3)
t15 DBENB lo Delay after STROBE lo		70		[1]
t16 DBENB Hold from STROBE hi	0			[1]

NOTE 1 For CPU generated MEMWB, data will appear about the same time as the STROBE, but for DMA generated MEMWB, data will appear before MEMWB.

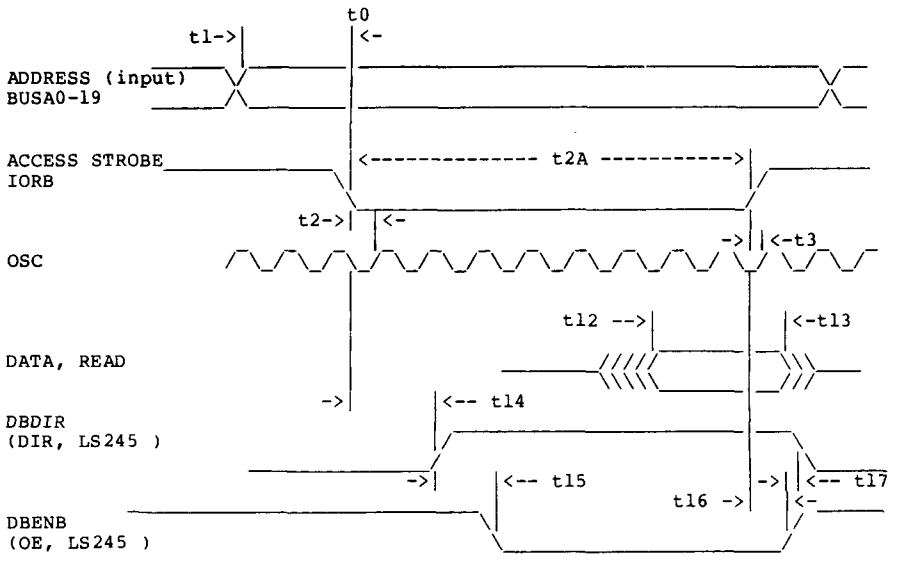


Figure 3. I/O CHIP SELECT PARAMETERS, READ

I/O CHIP SELECT PARAMETERS, READ

	min	typ	max	
t1 ADDRESS Valid Setup to STROBE lo	50			
t2 STROBE lo Setup to OSC hi	15			
t2A STROBE lo Length	420			
t3 STROBE hi Setup to OSC hi	20			
t12 DATA Valid Setup to STROBE hi	90			
t13 DATA Hold from STROBE hi	0			
t14 DBDIR hi Delay from STROBE lo			70	
t15 DBENB lo Delay after DBDIR hi		70		NOTE 1
t16 DBENB Hold from STROBE hi	0			
t17 DBDIR Hold after DBENB hi	0			NOTE 1

NOTE 1 ENable should be removed first before changing DIRection.

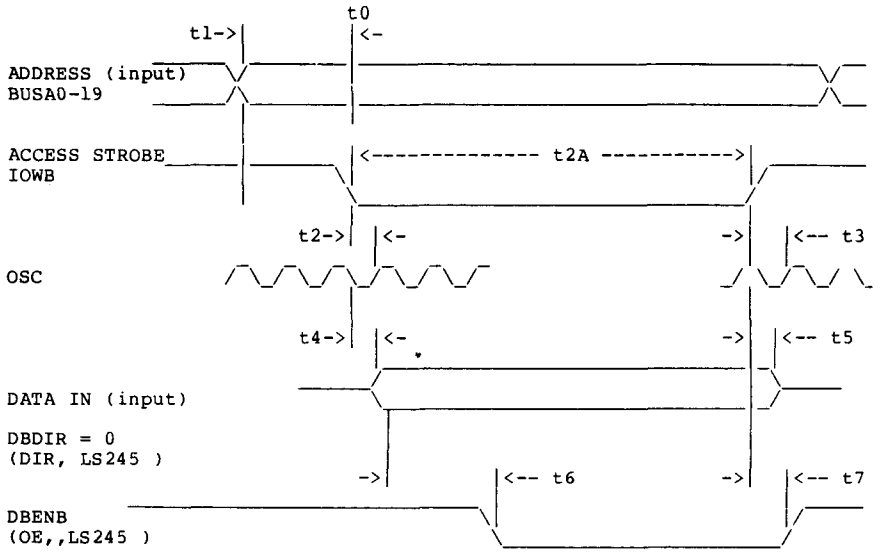


Figure 4. I/O CHIP SELECT PARAMETERS, WRITE

I/O CHIP SELECT PARAMETERS, WRITE

		min	typ	max
t1	ADDRESS Valid Setup to STROBE lo	50		
t2	STROBE lo Setup to OSC hi	15		
t2A	STROBE lo Length	420		
t3	STROBE hi Setup to OSC hi	20		
t4	DATA Valid Setup to STROBE lo		0	
t5	DATA Hold from STROBE hi	0		
t6	DBENB Delay after STROBE lo			70
t7	DBENB Hold from STROBE hi	0		

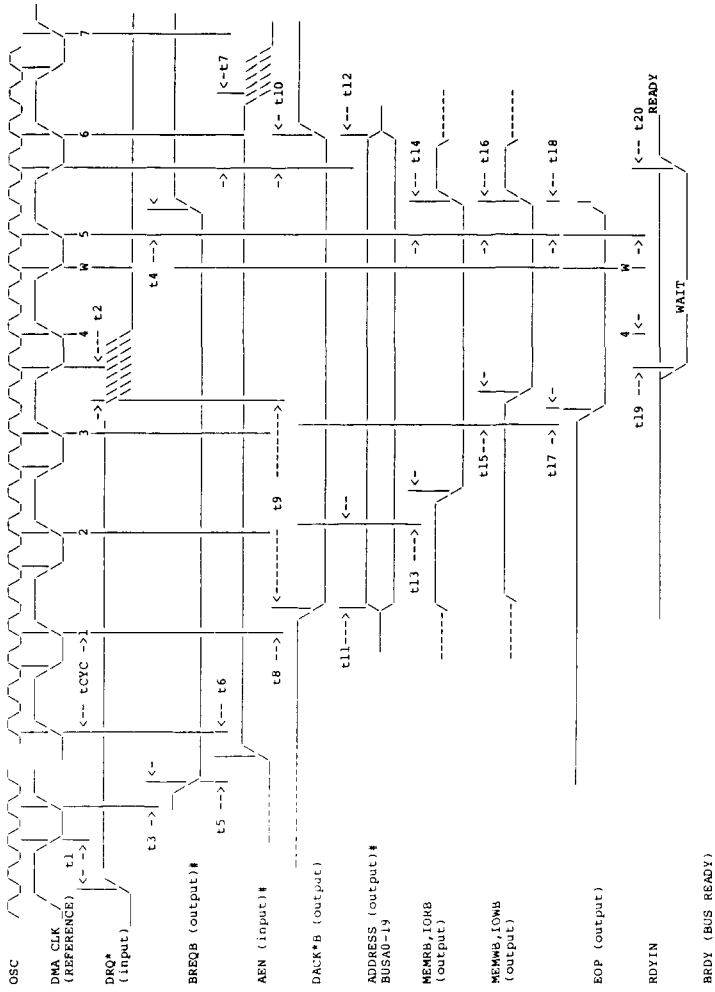


Figure 5. DMA BUS MASTER TIMING, READ / WRITE

DMA BUS MASTER TIMING, READ / WRITE

	min	typ	max	
t1 DRQ* True Setup to CLK lo	30			
t2 DRQ* False Setup to CLK lo	30			
t3 BREQB True Delay from CLK hi			120	8237A-5 tDQl
t4 BREQB False Delay from CLK hi			120	8237A-5 tDQl
t5 AEN True Delay after BREQB True	N x tCYC		+30	N =
t6 AEN True Setup to CLK Hi			40	
t7 AEN False delay from CLK hi			40	
t8 DACK*B True Delay from CLK lo			170	8237A-5 tAK
t9 DACK*B True Hold from AEN True	0			8237A-5 NOTE 6
t10 DACK*B False delay from CLK lo			170	8237A-5 tAK
t11 ADDRESS Valid Setup to CLK Hi	50			System Spec
t12 ADDRESS False delay from CLK hi	0			
t12 MEMRB or IORB True Delay from CLK hi			40	
t13 MEMRB or IORB False Delay after CLK hi			40	
t14 MEMWB or IOWB True Delay from CLK hi			40	
t15 MEMWB or IOWB False Delay after CLK hi			40	
t16 EOP True Delay after CLK hi			40	
t17 EOP False Delay after CLK hi			40	
t18 BRDY False Setup to CLK hi	30			
t19 BRDY False Hold after CLK hi	30			

PRINTER INTERFACE SPECIFICATION

PRINTER INTERFACE SPECIFICATION
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PRINTER INTERFACE SPECIFICATION
TANDY PART # 8075068
APRIL 30, 1986

1. GENERAL DESCRIPTION

1.1 The Tandy part# 8075068 - Printer Interface I.C provides the interface between the system I/O bus and the printer. Figure 1 shows Block diagram of Printer Interface chip. Figure 2 shows pin configurations of Printer interface chip.

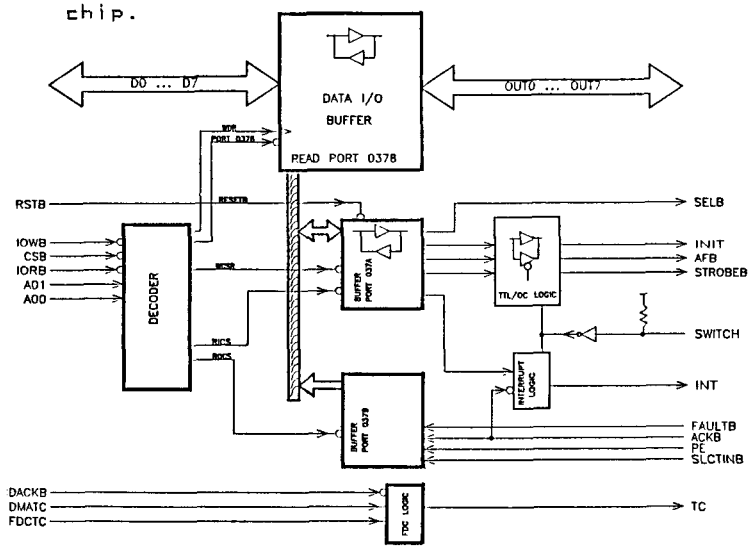


Figure 1.

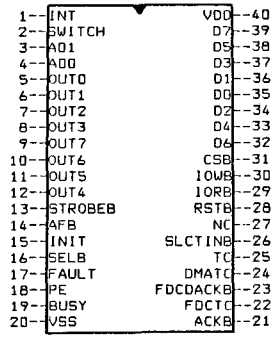


Figure 2.

1.2 DESCRIPTION OF EACH PINS:

Pin#	Pin Name	Type	Description
1	INT	output	Interrupt signal
2	SWITCH	input	Switch for totem pole output or open collector output on INITB, AF, STROBEB.
3	A01	input	CPU address line
4	A00	input	CPU address line
5	OUT0	input/output	Data I/O line
6	OUT1	input/output	Data I/O line
7	OUT2	input/output	Data I/O line
8	OUT3	input/output	Data I/O line
9	OUT7	input/output	Data I/O line
10	OUT6	input/output	Data I/O line
11	OUT5	input/output	Data I/O line
12	OUT4	input/output	Data I/O line
13	STROBEB	output	Printer Strobe signal
14	AFB	output	Printer Autofeed signal
15	INITB	output	Printer Initialize signal
16	SEL	output	Printer Select signal
17	FAULTB	input	Printer Fault signal
18	PE	input	Printer Paper empty signal
19	BUSY	input	Printer Busy signal
20	VSS	ground	Ground
21	ACKB	input	Printer Acknowledge signal
22	FDCTC	input	FDC Terminal Count
23	FDCDACKB	input	FDC-DMA Acknowledge signal
24	DMATC	input	DMA Terminal Count
25	TC	output	FDC Terminal Count signal
26	SLCTINB	input	Printer Select input
27	NC	--	Not used
28	RSTB	input	System Reset
29	IORB	input	CPU I/O Read strobe
30	IOWB	input	CPU I/O Write strobe
31	CSB	input	Chip select signal
32	D6	Input/output	CPU Data I/O
33	D4	Input/output	CPU Data I/O
34	D2	Input/output	CPU Data I/O
35	D0	Input/output	CPU Data I/O
36	D1	Input/output	CPU Data I/O
37	D3	Input/output	CPU Data I/O
38	D5	Input/output	CPU Data I/O
39	D7	Input/output	CPU Data I/O
40	VDD	power	+5 Volt Power Supply

2. ENVIRONMENTAL SPECIFICATIONS

2.1 Storage Temperature -65 C to 150 C
2.2 Operating Temperature 0 C to 70 C

3. ELECTRICAL SPECIFICATIONS

3.1 Absolute Maximum Rating

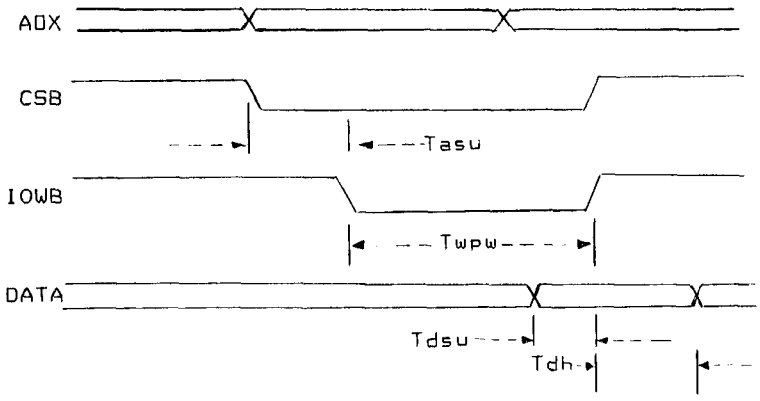
Parameter	Min.	Typ.	Max.	Units	Cond.
Voltage, any pin	-1.0		7.0	Volts	W.R.T ground
Power Dissipation			0.5	Watts	

3.2 D.C. Electrical Characteristics

Symb.	Parameter	Min.	Typ.	Max.	Units	Cond.
VDD	Supply Voltage	4.5	5.0	5.5	Volts	
Icc(q)	Quiescent current			50	uA	
Icc(o)	Operating Current			40	mA	
Vil	Input Low Voltage			0.8	Volts	TTL inputs
Vih	Input High Voltage	2.0			Volts	TTL inputs
Iin	Input Leakage	-10		10	uA	
Cin	Input Capacitance			7	pF	
Vol	Output Low Voltage			0.4	Volts	@4 mA
Voh	Output High Voltage	2.4			Volts	@-2 mA
Ioz	High Impedance Leak	-10		10	uA	

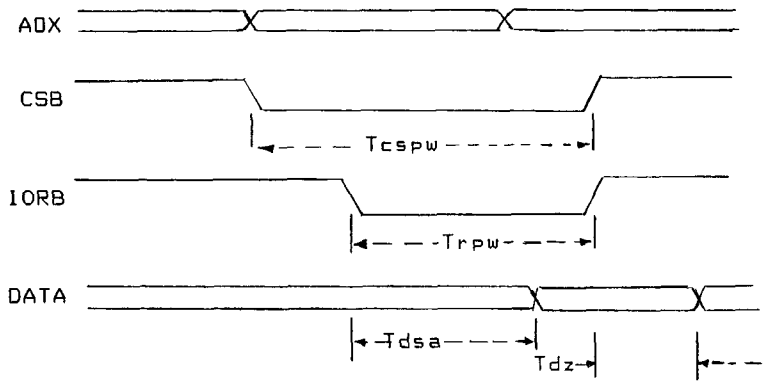
3.3 A.C Electrical Characteristics

3.3.1 Write Cycle



Symb.	Parameter	Min.	Typ.	Max.	Units	Cond.
Tasu	Address Setup	15			nS	
Twpw	Write Pulse Width	69			nS	
Tdsu	Data Setup	29			nS	
Tdh	Data Hold	6			nS	

3.3.2 Read Cycle



Symb.	Parameter	Min.	Typ.	Max.	Units	Cond.
Tcspw	Chip Select Width	69			nS	
Trpw	Read Pulse Width	69			nS	
Tda	Data Access			69	nS	
Tdz	Bus Hold/release	6		25	ns	

KEYBOARD INTERFACE SPECIFICATION

KEYBOARD INTERFACE SPECIFICATION
CONTENTS

GENERAL DESCRIPTION.....1
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KEYBOARD INTERFACE SPECIFICATION
TANDY PART # 8075069
MAY 05, 1986

1. GENERAL DESCRIPTION

1.1 The Tandy part# 8075069 - Keyboard Interface I.C provides two functions:

a. Interface between the system I/O bus and keyboard.

b. FDC support logic that generates DRIVE SELECT SIGNAL, MOTOR ON SIGNAL, FDC TERMINAL COUNT, FDC RESET and DMA/I.

Figure 1. shows block diagram of Keyboard Interface chip
Figure 2. shows pin configuration of Keyboard Interface chip.

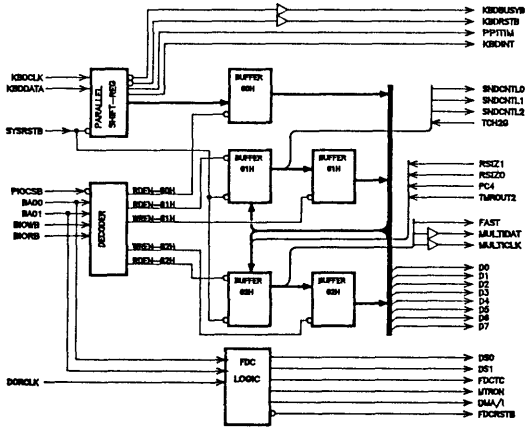


Figure 1.

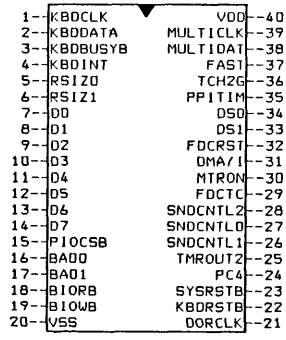


Figure 2.

1.2 DESCRIPTION OF EACH PINS:

Pin#	Pin Name	Type	Description
1	KBDCLK	input	Keyboard clock
2	KBDDATA	input	Keyboard data
3	KBDBUSYB	output	Keyboard busy signal
4	KBDINT	output	Keyboard interrupt signal
5	RSIZ0	input	Monochrome/color monitor mode
6	RSIZ1	input	Reserved
7	D0	input/output	Data I/O line
8	D1	input/output	Data I/O line
9	D2	input/output	Data I/O line
10	D3	input/output	Data I/O line
11	D4	input/output	Data I/O line
12	D5	input/output	Data I/O line
13	D6	input/output	Data I/O line
14	D7	input/output	Data I/O line
15	PIOCSB	input	Chip select strobe
16	BA00	input	CPU address line
17	BA01	input	CPU address line
18	BIORB	input	CPU I/O read strobe
19	BIOWB	input	CPU I/O write strobe
20	VSS	ground	Ground
21	DORCLK	input	Decode latch clock
22	KBDRSTB	output	Keyboard reset signal
23	SYSRSTB	input	System reset signal
24	PC4	input	Video memory size mode
25	TMROUT2	input	Timer counter from 8253 out2
26	SNDCNTL1	output	Sound control 1
27	SNDCNTL0	output	Sound control 0
28	SNDCNTL2	output	Sound control 2
29	FDCTC	output	FDC terminal count
30	MTRON	output	Motor ON signal to disk drive
31	DMA/I	output	DMA Request & FDC Interrupt enable
32	FDCRSTB	output	FDC reset signal
33	DS1	output	Drive select 1 signal
34	DS0	output	Drive select 0 signal
35	PPITIM	output	Timer Video signal
36	TCH2G	output	Timer channel 2 gate
37	FAST	input	4.77Mhz or 7.16Mhz mode select
38	MULTIDAT	output	Multi-data
39	MULTICLK	output	Multi-clock
40	VDD	power	+5 Volt Power Supply

2. ENVIRONMENTAL SPECIFICATIONS

2.1 Storage Temperature -65 C to 150 C
2.2 Operating Temperature 0 C to 70 C

3. ELECTRICAL SPECIFICATIONS

3.1 Absolute Maximum Rating

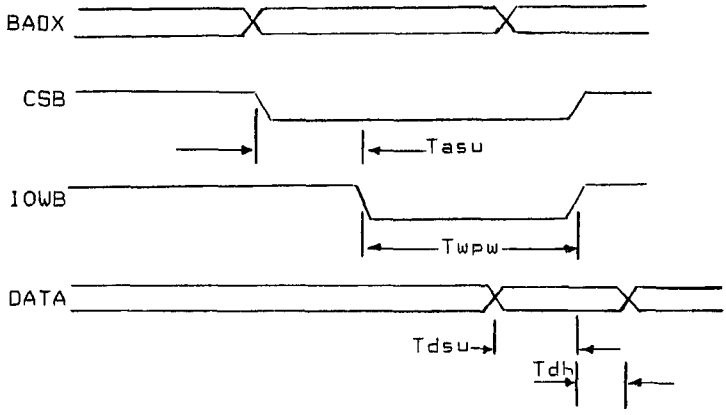
Parameter	Min.	Typ.	Max.	Units	Cond.
Voltage, any pin	-1.0		7.0	Volts	W.R.T ground
Power Dissipation			0.5	Watts	

3.2 D.C. Electrical Characteristics

Symb.	Parameter	Min.	Typ.	Max.	Units	Cond.
VDD	Supply Voltage	4.5	5.0	5.5	Volts	
Icc(q)	Quiescent current			50	uA	
Icc(o)	Operating Current			40	mA	
Vil	Input Low Voltage			0.8	Volts	TTL inputs
Vih	Input High Voltage	2.0			Volts	TTL inputs
Iin	Input Leakage	-10		10	uA	
Cin	Input Capacitance			7	pF	
Vol	Output Low Voltage			0.4	Volts	@4 mA
Voh	Output High Voltage	2.4			Volts	@-2 mA
Ioz	High Impedance Leak	-10		10	uA	

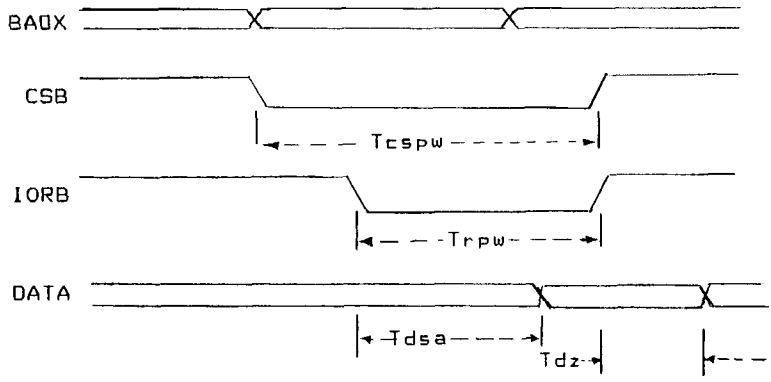
3.3 A.C Electrical Characteristics

3.3.1 Write Cycle



Symb.	Parameter	Min.	Typ.	Max.	Units	Cond.
Tasu	Address Setup	15			nS	
Twpw	Write Pulse Width	69			nS	
Tdsu	Data Setup	29			nS	
Tdh	Data Hold	6			nS	

3.3.2 Read Cycle



Symb.	Parameter	Min.	Typ.	Max.	Units	Cond.
Tcspw	Chip Select Width	69			nS	
Trpw	Read Pulse Width	69			nS	
Tda	Data Access			69	nS	
Tdz	Bus Hold/release	6		25	ns	

TIMING CONTROL GENERATOR

TIMING CONTROL GENERATOR
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TIMING DIAGRAMS

TIMING CONTROL GENERATOR
TANDY PART # 8075306
MAY 07, 1986
REV 050886

1.0 GENERAL DESCRIPTION

1.1 The Tandy part # 8075306 - Timing Control Generator:

- creates eight clock outputs from two independent oscillator inputs.
- synchronizes the ready signals.
- synthesizes the system control strobes from the CPU status signals.
- interfaces the system signals (HOLD, HLDA) with the CPU signals (RQ/GT).
- creates two FDC chip selects and the DMA request delay.

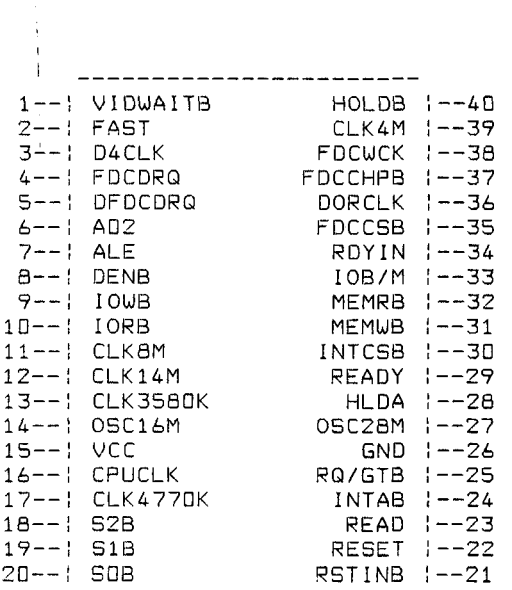
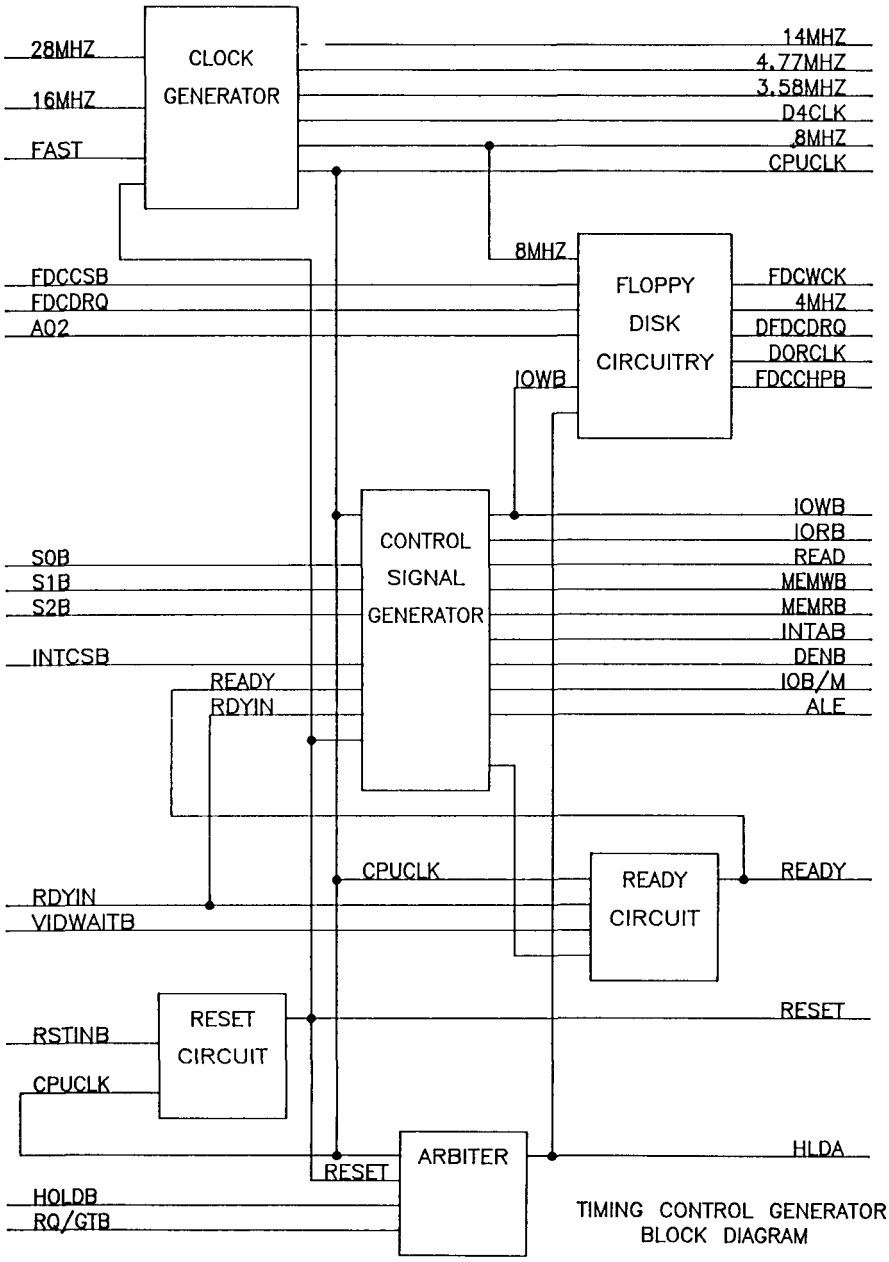


Figure 1. Pin Assignment

1.2 DESCRIPTION OF PINS:

Pin #	Pin Name	Type	Description
1	VIDWAITB	INPUT	Wait signal from video system (0 = Wait)
2	FAST	INPUT	Clock speed select
3	D4CLK	OUTPUT	CLK477M/4, Squarewave
4	FDCDRQ	INPUT	FDC DMA Request
5	DFDCDRQ	OUTPUT	Beginning of FDCDRQ delayed 1.0 microsec
6	A02	INPUT	System Address
7	ALE	OUTPUT	Address Latch Enable
8	DENB	OUTPUT	Data Enable
9	IOWB	OUTPUT	I/O Write
10	IORB	OUTPUT	I/O Read
11	CLK8M	OUTPUT	OSC16M/2, Squarewave
12	CLK14M	OUTPUT	OSC28M/2, Squarewave
13	CLK3S80K	OUTPUT	OSC28M/8, Squarewave
14	OSC16M	INPUT	Input Frequency = 16.00000 MHz
15	VDD	POWER	
16	CPUCLK	OUTPUT	FAST=1, CPUCLK=7.16MHz (OSC28M/4, 50-50 cycle) FAST=0, CPUCLK=4.77MHz (OSC28M/6, 33-67 cycle)
17	CLK4770K	OUTPUT	CLK14M/3, 33% duty cycle
18	S2B	INPUT	8088 Status Signal
19	S1B	INPUT	8088 Status Signal
20	S0B	INPUT	8088 Status Signal
21	RSTINB	INPUT	Asynchronous system input
22	RESET	OUTPUT	8088 CPU Reset input
23	READ	OUTPUT	Directional Control for CPU Data buffer
24	INTAB	OUTPUT	Interrupt Acknowledge
25	RQ/GTB	INPUT/OUTPUT	Request/Acknowledge/Release
26	VSS	GROUND	
27	OSC28M	INPUT	Input frequency = 28.63636 MHz
28	HLDA	OUTPUT	Bus Acknowledge
29	READY	OUTPUT	8088 CPU READY input
30	INTCSB	INPUT	8257 Interrupt Controller Chip Select
31	MEMWB	OUTPUT	Memory Write
32	MEMRB	OUTPUT	Memory Read
33	IOB/M	OUTPUT	1 = Memory access, 0 = I/O access
34	RDYIN	INPUT	Asynchronous system input (0 = Wait condition)
35	FDCCSB	INPUT	Previously decoded FDC Function I/O chip select
36	DORCLK	OUTPUT	Configuration register Chip Select
37	FDCCHPB	OUTPUT	FDC Chip Select
38	FDCWCK	OUTPUT	Pulse, Period = 2 microsec, 250(nom) pulse
39	CLK4M	OUTPUT	OSC16M/4, Squarewave
40	HOLDB	INPUT	Bus Request



TIMING CONTROL GENERATOR BLOCK DIAGRAM

2.0 ENVIRONMENTAL SPECIFICATIONS

2.1 Storage Temperature: -65 min, +150 max degrees C
2.2 Operating temperature: 0 min, +25 typ, + 70 max degrees C

3.0 ELECTRICAL SPECIFICATIONS

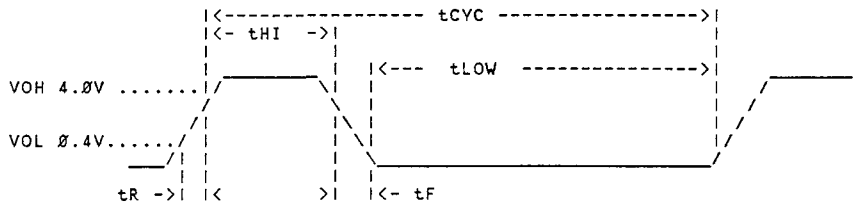
3.1 Absolute Maximum Rating:
Voltage on any pin w.r.t. Ground: -0.5 min, 7.0 max volts

3.2 Operating Electrical Specifications:

	min	typ	max	units
3.2.1 Operating Ambient:				
Air Temp. Range	0	25	70	degrees C
3.2.2 Power Supplies:				
VDD	4.5	5.0	5.5	volts
VSS	0	0	0	volts
ICC			100	milliamps
Total Power			700	milliwatts
3.2.3 Leakage Current, All Inputs:				
Vin = 0.0 v			-10	microamps
Vin = 5.0 v			+10	microamps
3.2.4 Input voltages:				
Logic "0"			.8	volts
Except RSTIN			.5	volts
Logic "1"	2.0			volts
Except RSTIN	3.5			volts
3.2.5 Output Voltages:				
logic "0" @ 4.0 mA load			.4	volts
logic "1" @ 4.0 mA load	2.4			volts
except all clocks	4.0			volts
3.2.6 INPUT CAPACITANCE (0.0 < Vin < 5.0)				
All inputs			10	pf
3.2.7 OUTPUT CAPACITANCE				
All loads			50	pf

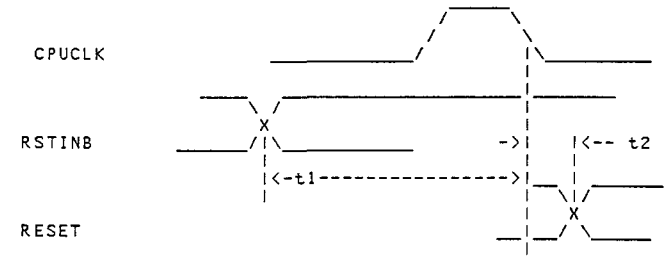
TIMING DIAGRAMS

FIGURE 1. CPUCLK



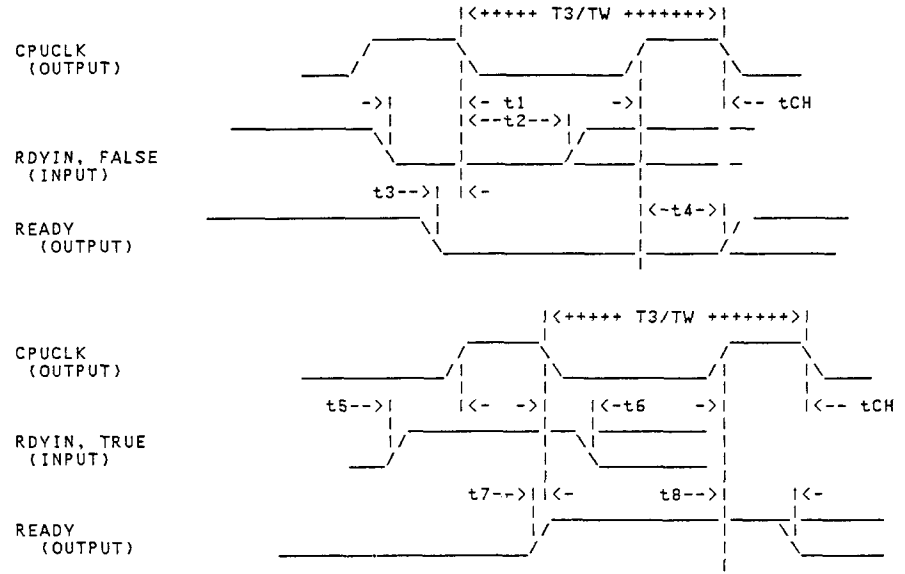
CLOCK PARAMETER	7.16 MHZ			4.77MHZ			
	min	typ	max	min	typ	max	
tHI Level at least 4.Øv	44	(69.5-tR-tF)		69	69.5		ns
tLOW Level not greater than Ø.4v	68	69.5		118	(14Ø-tR-tF)		ns
tR Rise time , Ø.4 to 4.Øv			8			1Ø	ns
tF fall time , 4.Ø to Ø.4v			7			1Ø	ns
tCYC		14Ø			21Ø		ns

FIGURE 2. RESET



RESET PARAMETERS	
t1 RSTIN Setup to CPUCLK low	Asynchronous input
t2 RESET Delay from CPUCLK low	4Ø ns max

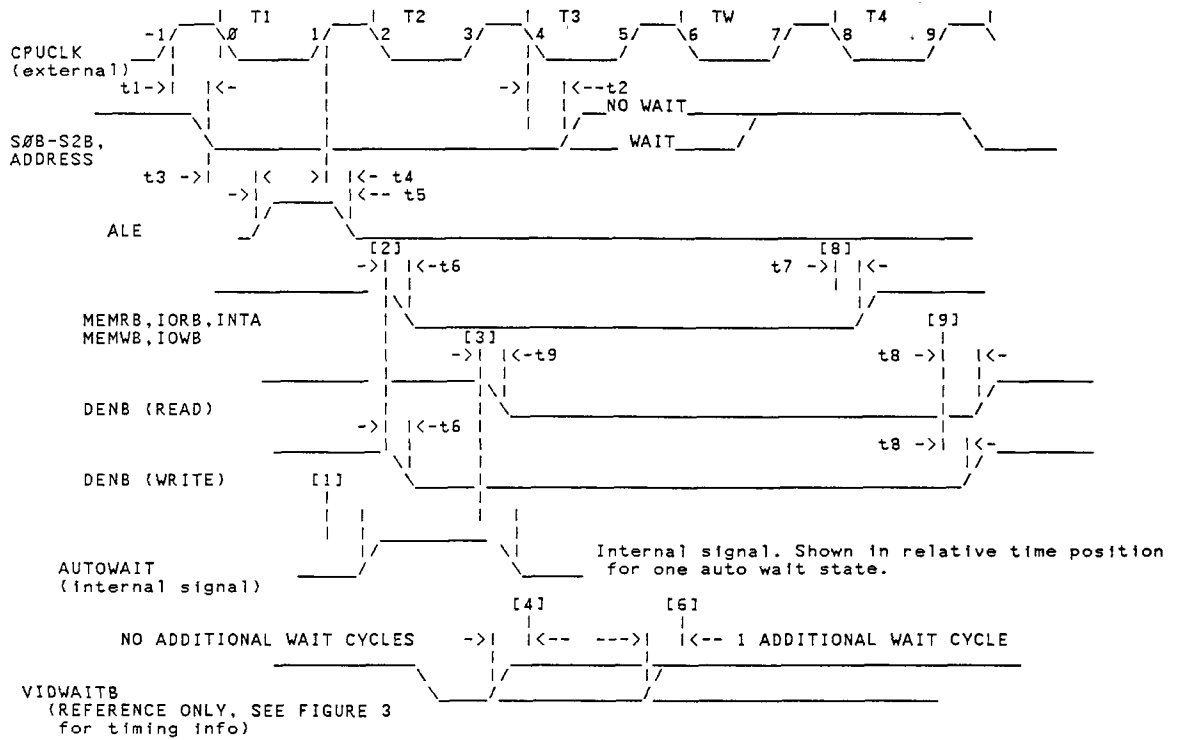
FIGURE 3. READY



READY PARAMETER

	min	max			
t1	RDYIN False Setup to CPUCLK low	35		ns	
t2	RDYIN False Hold after CPUCLK low	10		ns	
t3	READY False before CPUCLK low	-8		ns	tRYLCL 8088
t4	READY False Hold after CPUCLK hi		tCH + 8	ns	tCHRYX 8088
t5	RDYIN True Setup to CPUCLK hi	35		ns	
t6	RDYIN True Hold after CPUCLK low	10		ns	
t7	READY True before CPUCLK low	0		ns	tRYHCH 8088
t8	READY True Hold after CPUCLK hi		tCH + 8	ns	tCHRYX 8088

FIGURE 4. CONTROL GENERATOR



CONTROL GENERATOR

	min	max		
t1 STATUS Active Delay from CLK hi	1Ø	6Ø	ns	tCHSV 8Ø88
t2 STATUS Inactive Delay from CLK low	1Ø	7Ø	ns	tCLSH 8Ø88
t3 ALE True Delay from Status Active		2Ø	ns	tSVLH 8288

t4 ALE False Delay from CLK hi		2Ø	ns
t5 ALE Pulse Width	55		ns
t6 STROBE True Delay from CLK low		3Ø	ns
t7 STROBE False Delay from CLK low		3Ø	ns
t8 STROBE False Delay from CLK hi		3Ø	ns
t9 STROBE True Delay from Clk hi		3Ø	ns

FIGURE 5A. ARBITTER/REQUEST

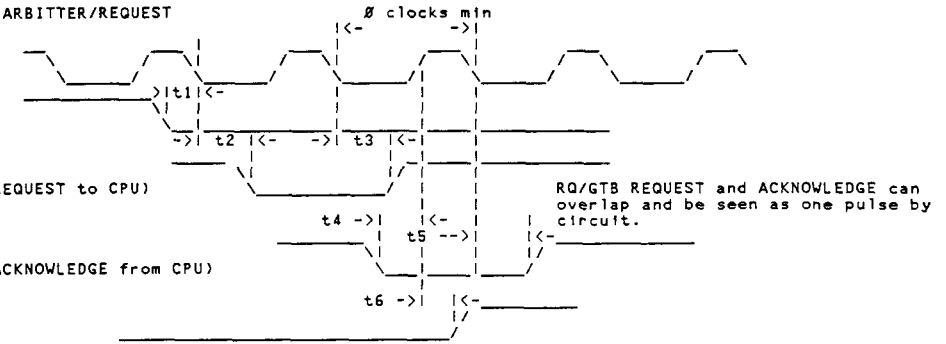
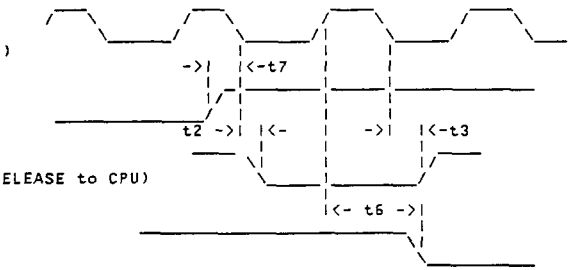


FIGURE 5B. ARBITTER/RELEASE

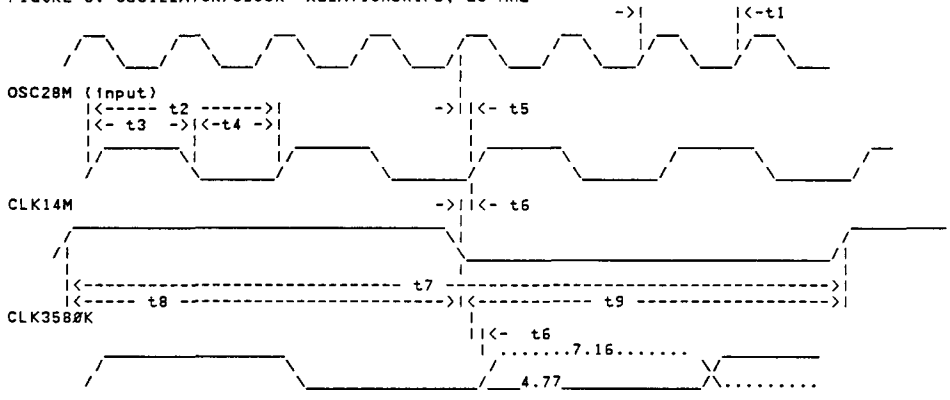


ABRITTER PARAMETER

	min	max		
t1 HOLDB (True) setup to CPUCLK low	2Ø		ns	
t2 CPUCLK low to RQ/GTB active (REQ/REL pulse)		5Ø	ns	tGVCH 8Ø88

t3 CPUCLK low to RQ/GTB inactive (REQ/REL pulse)		5Ø	ns	tCHGX 8Ø88
t4 RQ/GTB (True) setup to CPUCLK hi (ACK pulse)	2Ø		ns	tCLGL 8Ø88
t5 RQ/GTB (False) hold from CPUCLK low (ACK pulse)		5Ø	ns	tCLGH 8Ø88
t6 CPUCLK hi to HLDA Delay		3Ø	ns	
t7 HOLDB (False) Setup to CPUCLK low	2Ø		ns	

FIGURE 6. OSCILLATOR/CLOCK RELATIONSHIPS, 28 MHZ



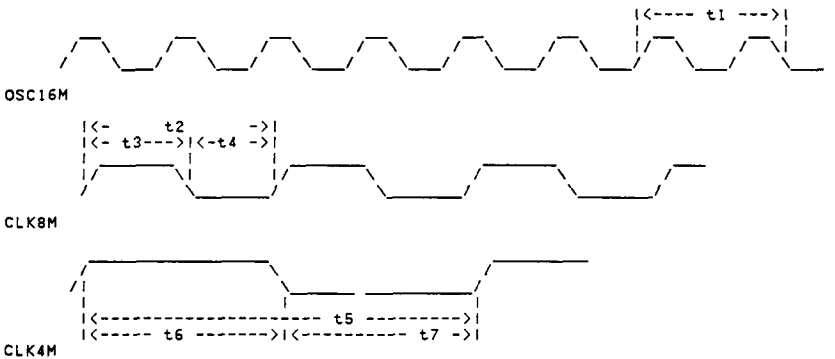
CLOCK PARAMETER	min	typ	max	
t1 OSC28M Period		34.9		NOTE 1
t2 CLK14M Period		t1 x 2		
t3 CLK14M high (includes tRISE)	-1Ø%	t2/2	+1Ø%	
t4 CLK14M low (includes tFALL)		(t2-t3)		
t5 OSC28M to CLK*M Output Delay skew		15		
t6 CLK*M to CLK*M Output Delay skew		15		
t7 CLK358ØK Period		t1 x 8		
t8 CLK358ØK high (includes tRISE)	-1Ø%	t7/2	+1Ø%	

t9 CLK3580K low (includes tFALL)	(t7-t8)	
tR CLK*M		10 ns
tF CLK*M		10 ns

NOTE 1 Use only one edge because the oscillator duty cycle symmetery can not be specified.

NOTE 2 Phase Relationship is important between the CLK14M clock and the outputs it generates.

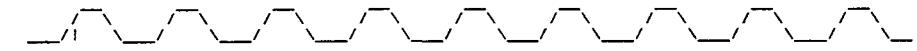
FIGURE 7. OSCILLATOR/CLOCK RELATIONSHIPS, 8MHZ



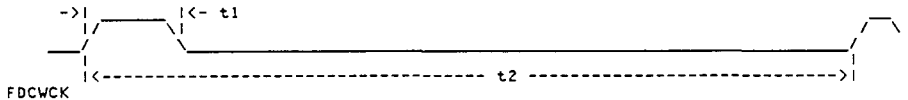
CLOCK PARAMETER	min	typ	max
t1 OSC16M Period		62.5	
t2 CLK8M Period		t1 x 2	
t3 CLK8M High (includes tRISE)	-10%	t2/2	+10%
t4 CLK8M Low (includes tFALL)		t2-t3	
t5 CLK4M Period		t1 x 4	
t6 CLK4M High (includes tRISE)	-10%	t5/2	+10%
t7 CLK4M Low (includes tFALL)		t5-t6	

tR		10 ns
tF		10 ns

FIGURE 8. FDCCLK/FDWCK RELATIONSHIPS



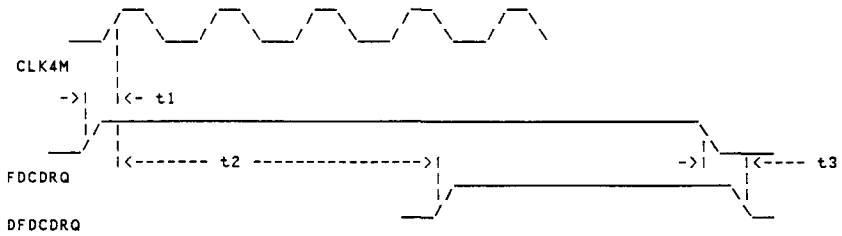
CLK4M (see FIG 7)



FDCWCK

CLOCK PARAMETER	min	typ	max	
t1 FDCWCK High (includes tRISE)		250		ns
t2 FDCWCK Period		2.0		us

FIGURE 9. CLK4M/FDDMAREQ RELATIONSHIPS



CLOCK PARAMETER					
	min	typ	max		
t1 FDCDRQ Setup to CLK4M	2Ø			ns	Asynchronous
t2 DFDCDRQ Delay TRUE	.75 us	1.Ø us	1.1 us		
t3 FDCDRQ False to DFDCDRQ False Delay			3Ø ns		